Grid converter for LED based intelligent light sources

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GRID CONVERTER FOR LED BASED INTELLIGENT LIGHT SOURCES

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ENERGY TECHNOLOGY
E.T.

Preface

This thesis is submitted in a partial fulfillment of the requirement for the Degree of Doctor of Philosophy. The work has been carried out at Aalborg University, Department of Energy Technology in cooperation with Martin Professional A/S. The project period was from September 2008 to September 2011.

During my research time much help was given by many people from the Department of Energy Technology and Martin Professional A/S. I would like to thank my supervisor Associate Professor Stig Munk-Nielsen, for his dedicated support and guidance in the field of power converters. I would like to thank also Carsten Karup Nielsen who helped and guided me in the hardware design and construction.

Thanks goes to industrial partners, Thomas Mansachs Frederiksen and Mikkel Holch, who helped me in power electronic design and in the field of digital controllers.

I would like to address my thanks to all the people at the Department of Energy Technology, who have followed and helped my research.

Aalborg, September 2011
M.Sc.EE Lajos Török

Summary

The purpose of this thesis was to investigate the applicability and effects of digital control to line connected switched mode power supplies with power factor correction. The main approach was cost effectiveness with high efficiency. This involved hardware design for increased switching frequency to reduce the size of the magnetic components. A description of different grid regulations was given followed by a set of converter topologies and controllers. Different control techniques were pointed out. Among the listed topologies and control solutions few were selected for further analysis, design and implementation.

Many of different hardware and control solutions available on the market were investigated. Most of the commercial power supplies are controlled by dedicated analog controllers in form an integrated circuit. Thus a survey was conducted to analyze the available state-of-art analog controllers and their implemented control algorithms. As digital control has to be competitive with the existing solutions it was investigated what digital signal processing solutions exist. A performance and cost comparison was also presented.

The chosen converter topologies were thoroughly analyzed. Different converters were chosen for different power levels. At low power simple boost converter as power factor corrector (PFC) and a RCD-clamped forward converter was chosen as DC-DC converter. This with has double output and coupled filter inductor. To design a digital controller with the tools of the classical control theory a small signal linearized model of the converter is needed. Detailed modeling and linearizing of the boost converter is presented.

At high power level interleaving technique is frequently used to reduce the current stress on the switching components. Though the number of magnetic components is increased they became smaller in size resulting in smaller current ripple through them. An interleaved boost converter with two legs is selected as PFC converter. It was shown that the small signal model of the interleaved converter is similar to the simple boost converter. Only the simple inductor has to be replaced by the paralleled inductors of each leg. This statement is valid only if the total inductor current is controlled rather than controlling the current in each leg. As second stage a phase-shifted full-bridge converter with synchronous rectification and current doubler was selected. It was shown that for output current and voltage control this topology can be modeled as a interleaved synchronous buck converter. As it can be seen interleaving technique is also present in this topology. For this topology a fuzzy logic voltage controller is proposed and compared to the traditional PI controller.

After modeling the converters controllers can be designed. The controller design was

interconnected with the hardware design and control platform. Thus two different prototypes were designed and built with two different digital controllers and the controller design, analysis and implementation was based on these two case studies.

The first prototype was a 70 W two-stage PFC and DC-DC converter with boost and forward converters. Average current mode control was selected, designed, simulated an implemented for the boost PFC converter. The two-loop control structure (fast internal current loop and lower bandwidth external voltage loop) was designed for nominal power but system behavior was also analyzed for low-load conditions. The controller was simulated in Matlab/Simulink using PLECS library and embedded Matlab function. All the parameters were treated and scaled just as they appear in the ADC interrupt of the 16 bit fixed point dsPIC30F1010 microcontroller. Peak current control was implemented for the forward converter, using analog comparator module of the digital-signal-controller. The waveforms, efficiency and power factor results were compared to the performance of an identical two stage 70 W power supply controlled with an analog PFC/PWM integrated circuit.

The second prototype was a 600 W two-stage PFC and DC-DC converter with interleaved boost and phase-shifted full-bridge (PSFB) converters. Average current mode control was designed simulated and implemented for both converters. The sum of the boost inductor current was controlled to shape the line current and the sum of the filter inductor currents in the PSFB converter was controlled to limit over-currents. Low bandwidth PI controllers control the boost DC and the output DC voltages. A fuzzy logic output voltage controller was also simulated and compared to the performance of the PI controller. All four control loops were implemented in a 16 bit fixed point dsPIC33FJ32GS406 microcontroller driving at the same time 8 PWM channels.

Finally a brief analysis was done on the effect of the grid disturbances, especially voltage sags on the digital controller. Different grid codes and compatibility requirements and system behavior through a boost converter with digital control was presented.

In this thesis a deep knowledge of design and digital control of line connected switched mode power supplies with power factor correction was gathered and appropriate solutions were presented. The advancement of this thesis will enable improved design and digital control of high frequency switched mode power supplies in the future. It is concluded that the digital signal processors available today are competitive in performance with the state-of-art analog ICs. The economic reasons for using digital control is not so clear but with falling prices of microcontrollers and increasing demands on the performance of power converters introducing digital control seems to be a reasonable option for the future development of power converters. Advanced control structures can be implemented to improve the performance of switched-mode power-supplies and power factor corrector circuits.

Main contributions of this work are:

- An investigation on the effect of the use of digital control in switch-mode power-supply applications.

- Development of a simulation platform in Matlab/Simulink using triggered embedded

Matlab functions to model digital control, suitable for different power converters with close to real life conditions.

- Digital signal processor-based control of four different power converter topologies with embedded low cost 16 bit fixed point microcontroller.
- Comparison of analog control and digital control of two identical 70W two-stage power factor corrector and DC-DC converters regarding cost effectiveness, power factor and efficiency.
- Digital fuzzy logic controller proposed for low bandwidth voltage control to high frequency switched-mode power supplies.
- Investigation on the effect of grid disturbances on the control of low-voltage-grid-connected power supplies.

Nomenclature

ΔD Duty cycle deviation due to the finite slope of the primary current

ΔI Inductor average-to-peak current ripple

Δi_L Inductor average-to-peak current ripple

ΔI_{Lf} Filter inductor peak-to-peak current ripple - in modeling of the PSFB converter

Δt Shift variation in the PSFB converter

Δv_o Output voltage ripple

η Efficiency

$\hat{d}$ Duty cycle perturbation

$\hat{d}_{eff}$ Effective duty cycle perturbation

$\hat{d}_i$ Duty cycle perturbation due to filter inductor variation

$\hat{d}_v$ Duty cycle perturbation due to input voltage variation

$\hat{i}_L$ Inductor current perturbation

$\hat{i}_o$ Output current perturbation

$\hat{i}_{L1}, \hat{i}_{L2}$ Interleaved boost inductors current perturbation

$\hat{i}_{Lf1}, \hat{i}_{Lf2}$ Filter inductor current perturbation

$\hat{i}_{Lp}$ Paralleled inductor voltage perturbation

$\hat{v}$ Output voltage perturbation

$\hat{v}_g$ Supply voltage perturbation

$\hat{v}_{L1}, \hat{v}_{L2}$ Interleaved boost inductor voltage perturbation values

$\hat{v}_{Lf1}, \hat{v}_{Lf2}$ Filter inductor voltage perturbation

$\hat{v}_{Lp}$ Paralleled inductor voltage perturbation

$\hat{v}_L$ Boost inductor voltage perturbation

ω_n Natural frequency

ω_{iz} Frequency of the zero

ω_{vz} Frequency of the zero

ζ Damping

C Filter capacitor

$C1, C2$ Half bridge capacitors

C_f Filter capacitor

C_b Blocking capacitor

$C_{internal}$ Internal capacitance of the converter components

Cdc Boost capacitor

Cf EMI filter capacitor

Co Forward filter capacitor

$cos\phi$ Displacement factor

D Duty cycle ($0 \leq D \leq 1$) - steady state value

D Switching diode

d Duty cycle instantaneous value

$D1, .., 4$ Bridge rectifier

D' 1-D - steady state value

d' 1-d

D_{eff} effective duty cycle of the PSFB Converter

D_{max} Maximum allowed duty cycle

d_{vmax} Saturation point of the voltage controller output, presented in Q.15 format

dev Voltage error variation

di_L Boost inductor current variation

di_{L1}, di_{L2} Interleaved boost inductor current variations

di_{Lf1}, di_{Lf2} Filter inductor current variations

dv Output voltage variation

e Controller input

e_i Current error

e_v Voltage error

ev Voltage error

Ext_ref Reference signal TL431 shunt regulator to the analog comparator

f_L Line frequency

f_S Switching frequency

G_{HALL} Hall-sensor gain

G_{id0} Current transfer function gain

G_{id} Duty cycle-to-inductor current transfer function

G_{ig} Input voltage-to-inductor current transfer function

G_{INA193} Amplifier gain

G_{sysv} Voltage loop transfer function

G_{vd0} Voltage transfer function gain

G_{vd} Duty cycle-to-output voltage transfer function

G_{vg} Input voltage-to-output voltage transfer function

Gm Gain margin

I integral component

I_C Capacitor current - Steady-state value

i_C Boost capacitor current

I_L Inductor current - Steady-state value

I_n n^{th} harmonic of the input current

I_o Output current - Steady-state value

I_1 The fundamental of the input current

i_{ds} Forward drain-source current

i_g Input current instantaneous value

I_{L1}, I_{L2} Interleaved boost inductor current - Steady-state values

I_{Lf1}, I_{Lf2} Filter inductor current - Steady-state values

I_{lf} Filter inductor current - Steady-state value

I_{load} Load current

I_{peak_L1}, I_{peak_L2} Interleaved boost inductor currents - peak values

I_p Peak value of the primary current

i_p Primary current

i_{ref} Current reference

I_{rms} The rms value of the input current

K Scaling factor

K_d Distortion factor

K_{dev} Error variation coefficient

K_{ev} Error coefficient

Ka Anti-windup coefficient

Ki Integral coefficient

Kii Current Ki coefficient

Kiv Voltage Ki coefficient

Kp Proportional coefficient

Kpi Current Kp coefficient

Kpv Voltage Kp coefficient

L Inductor

L_1, L_2 Interleaved boost inductors

L_C Critical inductance value

L_f Filter inductor

L_{lk} Leakage inductance of the PSFB transformer

L_m Magnetizing inductance of the PSFB transformer

L_p Paralleled interleaved boost inductors

Lf EMI filter inductor

$Lf1, Lf2$ Output filter inductors of the current doubler

Lo Forward filter inductor

M The peak value of the input current

M_p Maximum overshoot in %

n N_s/N_p

n_1, n_2 Number of turns in the primary and secondary windings

n_3 Number of turns in the secondary of the forward transformer

N_p, N_s Number of turns in the primary and secondary winding of the PSFB transformer

P Proportional component

PIi Current PI controller

PIv Voltage PI controller

Pm Phase margin

Po Output power

Q Switching MOSFET

QA, QB, QC, QD Full bridge MOSFETs

R Load resistance

R_{div} Voltage divider gain

R_{ids} Forward drain-source current measurement resistor

R_{iL} Inductor current measurement resistor

R_{inrush} Inrush protection thermistor

Rs, Cs, Ds RCD snubber resistor, capacitor and diode

$SR1, SR2$ Synchronous rectifier MOSFETs

T_s Switching period

T_{si} Current sampling time

T_{sv} Voltage sampling time

Tr Transformer

u Controller output

V Output voltage - Steady-state value

v Output voltage - instantaneous value

V_D Diode voltage drop

V_g Supply voltage - Steady-state value

v_g Supply voltage - instantaneous value

v_L Inductor voltage

V_o Output voltage - average value

V_{ac-min} Low line voltage rms value

V_{ac_meas} Measured rectified line voltage

V_{ac} AC voltage source

V_{dc_meas} Measured rectified line voltage

V_{max} maximum of the line voltage, presented in Q.15 format

V_{ref} Reference voltage

V_{rms} The rms value of the input voltage

Vdc DClink voltage, input voltage for the DC-DC converter

Vf Forward output voltage

Vf_{meas} Measured forward output voltage

Vp, Vs Voltages in the primary and the secondary winding of the PSFB transformer

$X(Q.15)$ measured value transfered to Q.15 value

$x_{measured}$ Measured value, sent to ADC converter

Z_b Factor including leakage inductance and switching frequency

Abbreviations

ADC Analog digital converter

ALU Arithmetical logical unit

CBEMA The Computer and Business Electronic Manufactures Association

CCM Continuous conduction mode

CM Common mode

CRM Critical conduction mode

DCM Discontinuous conduction mode

DKK Danish currency

DM Differential mode

DSP Digital signal processor

EMC Electromagnetic compatibility

EMI Electromagnetic interference

FOH First order hold

FPGA Field-programmable gate array

*ICD*2/3 In-circuit debugger

ITIC Information Technology Industrial Council

PCB Printed circuit board

PF Power factor

PFC Power factor correction

PLL Phase locked loop

$PSFB$ Phase-shifted full-bridge

PWM Pulse width modulation

rms Root-mean-square value of an alternating signal

$SEMI$ Semiconductor Equipment and Materials International

THD Total harmonic distortion

VCC Supply voltage of the analog controller

VDD dsPIC supply voltage

VEE dsPIC ground = primary ground

ZOH Zero order hold

ZVS Zero voltage switching

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Chapter 1

Introduction

This thesis was meant to present the advantages and disadvantages using digital signal processors in grid connected switched mode power supply applications. The aim is to show that digital controllers are competitive and cost effective in controlling most of the high frequency converters in comparison to the state-of-the-art analog controllers. Limitations for digital control like special types of converters and control methods are also highlighted.

1.1 Motivation

Recent developments in digital signal processor technology show a way of changing from analog controllers, which are widely used nowadays in power supply applications, to digital controllers. The cost of digital microprocessors has dropped in the last years [1]. Programming digital controllers in high level languages makes them easy to use: allows flexibility in control algorithm modifications without significant hardware changes. The absence of the phenomenon of aging and less thermal and noise sensitivity, present in analog controllers [2], is on the favor of digital solutions. Also the demand for system-module communication requires more sophisticated control platform than analog controllers. Beside the advantages of digital controllers there are many drawbacks like system integration, auxiliary power supply, discretizing and sampling errors, data transport delay, number representation etc... Also communication between system and module is getting an essential need in order to prevent faults and react in time with redundant elements in case of errors. All these issues together with the design of the power converters to suit the demands of digital control, different standards and requirements make an interesting research subject.

This work is part of the INLED (Intelligent Light Emitting Diodes) project and it has been carried out in cooperation with Martin Professional A/S and Aalborg University, Department of Energy Technology with the objective of investigating and developing grid converters for LED-based intelligent light sources. The project was co-funded by Højteknologifonden, Danmark. The objective of the project is to increase the knowledge in LED based luminaire technology and using this knowledge substitute the existing technologies. The project focuses on creating: optics with nano scale coatings that would maximize the light transmission from LED diodes to the output port, efficient power electronic drivers supplying power to the diodes and a heat management system for the

luminaire.

The term *intelligent lighting* means the ability to control position, beam, color-mixing of a lighting fixture. The products today use traditional technologies like discharge and incandescent lamps. A rapidly growing percentage of new products are based on LED technologies, due to some benefits of it: longer lifetime, potentially reduced energy usage, smaller size and weight. To power the LED a voltage of 4-6 V is required, obtained from the single phase grid (universal line voltage of 85V to 270V). The power consumed by the LEDs has to be converted in 3 power stages (PFC, step-down DC-DC and LED driver DC-DC converters), and each conversion step dissipates heat. In this project the AC-DC and DC-DC stages was optimized to minimize the material usage of EMI filter, magnetic components and cooling systems. To maintain system performance an increased level of semiconductors and signal processing was introduced. Digital control of the converters was implemented in embedded digital signal processors (DSP).

The thesis also presents the results of the research done in the SECURITAC project - 7th Framework Programme - High reliability, low cost, stackable power supply for security systems. Security systems (including fire, intrusion, access control, and voice alarm) typically contain an AC-DC power supply to deliver power to the system and to charge and maintain 12V batteries, which provide the *secondary source* during a mains failure. The combined power supply-charger-battery system represents a key component of such systems in terms of cost and contribution to system reliability. In addition, as amendments were made to the applicable EN standards (EN54-4/A2, EN50131-6, EN60849, etc) manufacturers are often required to re-design, re-test and re-certify each power supply design, which represents significant actual and opportunity costs. As such, the objective of this project was to address the costs associated with existing security system power supplies, and at the same time significantly improve the manufacturability, reliability and the feature set of these key components. The stackable (load sharing) approach offered increased reliability through design and redundancy and cooler operation by spreading component heat over a larger surface area. Manufacturing costs were minimized via the manufacture of high volumes of a common module to suit a wide product range.

1.2 Problem Formulation

The increased number of electrical equipment connected to the mains arise different potential side effects such as voltage distortion and pulsating, non-sinusoidal line currents causing functional disorders to other consumers and affecting the power distribution system. The most common malfunctions that can appear in power electrical systems are overheating of the components due to current distortion, fast deterioration of switching components, mechanical oscillations of motors, isolation failure due to possible over-voltages, audio noise and radio interferences. This is due to the nonlinear characteristic of the power circuits and loads [3]. The nonlinear loads need some power conditioning. To reduce the negative impacts of power electronic systems to the utility grids and their electrical environment the engineers have big responsibility to design the power conditioning circuits to prevent generating and distributing harmonic currents and reduce electro-magnetic interferences.

Not only designing but also controlling these power converters needs distinguished

attention. Although numerous integrated analog solutions exist the evolution of low-cost and high speed microprocessors makes digital control cost-effective and real possibility and opens new perspectives in controlling high frequency switched-mode power supplies. Also it have to be considered the recent needs for a human-machine interface, which allows the user to monitor the behavior of the equipment. This is impossible without involving microprocessors. To make digital control really competitive to analog controllers problems like integration of the microcontrollers, power consumption, metering errors at high speed sampling has to be investigated.

The first aim of the research project is:

- *To examine and compare the suitable topologies for digital control in order to have the required power conditionings: power factor correction, isolation and have the required nominal output power.*

In order to implement digital control there are different issues which have to be considered. Additional cost is one major issue which comprehends the price of digital controller and addition components compared to analog controllers, but also technical problems, like supply for the controller and auxiliary components (sensors, amplifiers, gate drivers) has to be taken into account. So, the second objective is

- *To investigate the technical and economical problems integrating digital controllers on-board a power converter. Is it feasible to replace analog controllers with digital controllers?*

Digital control, regardless how big the computational power of the controller is, it introduces errors in the real system due to PWM and sampling resolution and transport delay of the system. These errors have to be considered and compensated when designing the control algorithm. Therefore the third objective is:

- *To develop, implement and evaluate digital control firmware considering all challenges in digital control.*

Different limitations and regulations exist for grid connected converters from harmonic distortion (standards) to efficiency and stand-by operation mode (efficiency compliance regulations). Different components might influence the converter behavior such as magnetic components with core losses, saturation of the magnetic components, switching components with switching and conduction losses, the routing might introduce radiation. The converters needs to meet these regulations to be competitive with the market so the fourth objective is:

- *To analyze the converter efficiency from no-load condition to full power operation and identify the different loss sources.*

The increased demand for using the power supply network many times ends up in different unwanted events which can cause different deviations of the normal operation of the power grid - voltage sags, voltage fluctuations, frequency deviation etc.... In this condition grid connected power supplies have to be resistant to line faults. The last objective is:

- *To analyze the converter behavior in response to line faults and investigate different safety mechanisms.*

1.3 Contributions

- An investigation on the effect of the use of digital control in switch-mode power-supply applications was carried out. Controllers were designed for linearized discrete models of the power converters in discrete space and advantages and limitations such as processor speed, transport delay and sampling and PWM resolution were highlighted.

- A simulation platform was developed in Matlab/Simulink using triggered embedded Matlab functions to model digital control of different power converters with close to real life conditions.

- Digital signal processor-based control of four different converters (boost and interleaved boost PFC, forward and phase shifted full bridge DC-DC converters) with embedded processor to the main PCB was designed, built and tested. A low cost 16 bit fixed point dsPIC microcontroller was used, the firmware was written in C programming language. By scaling the measured data in a proper way, the algorithm can be implemented indifferent on the power level.

- Comparison of analog control and digital control of two identical 70W two-stage power facto corrector and DC-DC converters. The purpose was to investigate the cost effectiveness and efficiency of two stage PFC and DC/DC converters.

- Digital fuzzy logic voltage control proposed for output voltage regulation of a 600W phase-shifted full-bridge converter with synchronous rectification and current doubler. The designed controller shows better results in the system dynamics compared to a PI voltage controller using the same parameters. The Fuzzy algorithm was programmed in 16 bit fixed point dsPIC microprocessor.

- Analysis on the effect of grid disturbances on digitally controlled low-voltage-grid-connected power supplies.

1.4 Related Presentations and Publications

Parts of the work presented in the thesis were published in different conference proceedings and reports:

Lajos, Török; Stig, Munk-Nielsen - "Simple digital control of a two-stage PFC converter using dsPIC30F microprocessor" - PEMD 2010 - The 5th IET International Conference on Power Electronics, Machines and Drives - 2010, Brighton, United Kingdom

Lajos, Török; Stig, Munk-Nielsen - "Efficiency and hardware comparison of analog control-based and digital control-based 70 W two-stage power factor corrector and DC-DC converters" EPE 2011 - EPE 2011 - The 14th European Conference on Power Electronics and Applications - 2011, Birmingham, United Kingdom

Lajos, Török; Stig, Munk-Nielsen - "Digital Fuzzy logic and PI control of phase-shifted full-bridge current-doubler converter", - INTELEC 2011 - The International Telecommunications Energy Conference - 2011, Amsterdam, The Netherlands

Lajos, Török; Szymon, Beczkowski; Jesper, Gadegaard; Thøger, Kari; Stig, Munk-Nielsen; Kjeld, Pedersen - "High Output LED-Based Profile Lighting Fixture" -IECON 2011 - 37th Annual Conference of the IEEE Industrial Electronics Society - 2011, Melbourne, Australia

Last paper sent for review:
Lajos, Török; Stig, Munk-Nielsen - "Effect of voltage sags on digitally controlled line connected switched-mode power supplies" - 13th International Conference on Optimization of Electrical and Electronic Equipment - OPTIM 2012, Brasov, Romania

1.5 Outline

The document is collected into the following six chapters:

Chapter 1 Introduction is the chapter where the motivation, background and problem statement is presented. It contains also a brief description of the contributions and acknowledgment of the knowledge. Finally the outline of the individual chapters is given.

Chapter 2 Converters, controllers and control methods is the chapter where the related previous work is presented. It starts with presenting the limitations and regulations regarding connecting power converters to the grid. For different power levels different power converters are recommended. A brief description of these converters is included. A market survey has been carried out regarding analog and digital controllers for different power supply applications. Different manufacturers produce switched mode power supplies with active power factor correction, controlled either by analog either by digital controllers. A market survey is presented also on this topic. To be able to implement an embedded power converter and controller system, auxiliary power supplies are required for the controller. Different solutions were investigated and presented in this chapter. The last part presents different control strategies suitable and less suitable for digital implementation.

Chapter 3 Digital control design presents the design requirements for digital control. It starts with the modeling of the power converter, in order to analyze its frequency behaviors. Discretizing the continuous model and the digital control itself it bears some challenges: the inadequate sampling frequency might introduce unexpected sampling errors, different digital controllers have different ADC and PWM resolutions resulting in quantization error. The delay between the calculation and updating of the duty cycle register also influences the the control stability. These challenges are presented within this chapter. The final part part describes the control design procedure: requirements for selecting the right control bandwidth, the characteristics of a fast current and a low bandwidth voltage loop design.

Chapter 4 Digital control in application presents a case study on two different power converters. A 70W two-stage PFC and DC-DC converter and a 600W two-stage PFC and DC-DC converter. Both with embedded digital controller. The 70W power supply is compared with an identical but analog controller driven one.

Chapter 5 The influence of grid disturbances on switched-mode power supplies describes different grid disturbances, analysis the grid codes and different requirements regarding switch mode power supplies. Also PFC converter control issues and dynamic behavior is presented.

Chapter 6 Conclusions and future work, is the chapter which concludes the work, points out the main contributions and suggests opportunities for future works.

Chapter 2

Converters, controllers and control methods

To supply any electrical equipment connected to the grid some power conditioning circuits are needed. These circuits and loads have highly nonlinear characteristics. The following chapter will present the different regulations that limit the line current and voltage distortion caused by the nonlinear loads and discuss upon a series of power factor corrector and DC-DC converter topologies and control strategies that are suitable for digital implementation. Also a market survey was carried out to present different analog and digital controllers.

The simplest power conditioning circuit with the worst characteristic is the single-phase diode rectifier with capacitive output voltage filter (Figure 2.1 a.)). The AC side is influenced by the network impedance, the DC side ripple is determined by the filtering capacitor [5]. The line current is polluted with odd harmonics, the amplitude of the 3^{rd}, 5^{th}, 7^{th} and 9^{th}order harmonics are significant (Figure 2.1 b.)).

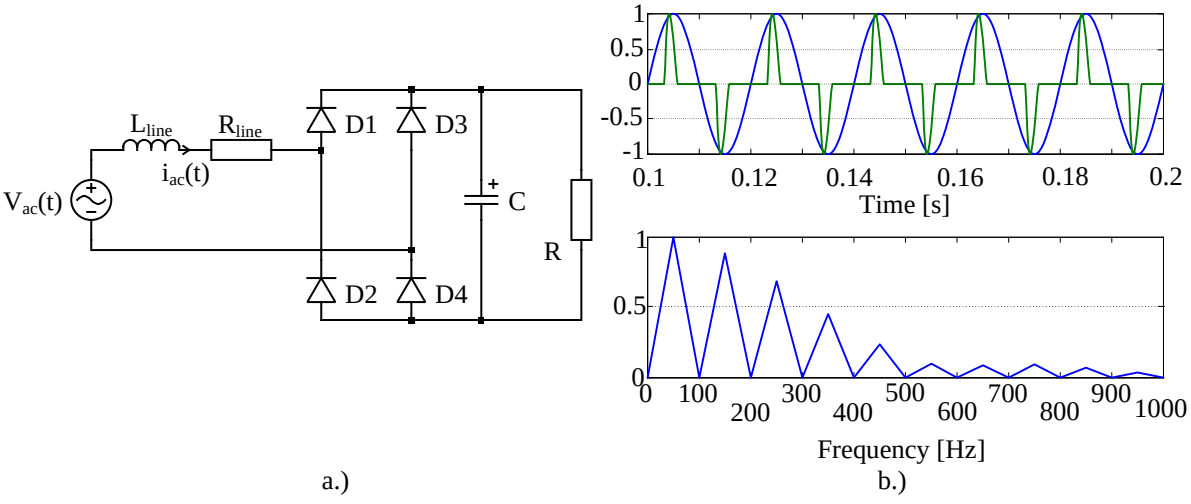


Figure 2.1: *Capacitive filtered single-phase diode rectifier a.) Schematic b.) Waveforms - Top: Blue - Normalized line voltage, Green - Normalized line current; Bottom: Normalized Line current spectrum*

2.1 International standards

To overcome the problems caused by the current distortion and limit the line current harmonics different national and international standards were released. In the United States in 1981 was introduced standard IEEE-519-1981 with name: *'IEEE guide for harmonic control and reactive compensation of static power converters'* which deals only with voltage fluctuations. This was updated in 1992 to ANSI/IEEE-519-1992, *'IEEE recommended practices and requirements for harmonic control in electrical power systems*, which determines limits to voltage fluctuations and also current harmonics [6].

The International Electrotechnical Committee in 1982 published three-part standard IEC 555: part 1 - Definitions, part 2 - Harmonics [7], part 3 - Voltage fluctuations, which was later adopted by the European Committee for Electrotechnical Standardization as DS/EN 60555. In 1995 standard IEC 555 became part of the IEC 1000 standard family (respectively DS/EN 61000 standard family) and Part 3 of it considering limits of voltage and current harmonics.

Standard IEC 61000-3-2 is applied to to electrical equipment with an input current lower or up to 16 A_{rms} per phase which are intended to be connected to low voltage (single phase 50 Hz system with 220-240 V_{rms} and three phase systems with 380-415 V_{rms}) power distribution system. The standard limits the harmonic content of the injected currents to the supply system. The electrical equipment are classified in four groups (**A**,**B**,**C**, and **D**) [8].

Class **A** includes balanced three phase equipment, audio equipment, but excludes those equipment identified as belonging to Class **D**. The harmonic limits of the input current for Class **A** should not exceed the absolute values in given in table from Figure 2.3

Class **B** includes portable tools, non-professional arc welding equipment. The limits of the input current harmonics are shown in table from Figure 2.3 multiplied by a factor of 1.5

Class **C** includes lightning equipment. For lighting equipment the limit for input harmonic currents is shown in Figure 2.4

Equipment included in Class **D** should have a special input current shape and an active power $P \leq 600W$ (Figure 2.2). The limits for input harmonics are presented in table from Figure 2.5 The input current shape should fit in the envelope, presented in Figure 2.2, in every half period in 95%. So if the current has small peaks outside the envelope the equipment can be considered as class D equipment. The center line M coincide with the peak value of the input current [8]. The current wave shape presented in Figure 2.2 can be achieved with open loop fixed duty cycle switching or simply turning off the switching devices in the middle of the interval. This will result in reduced switching losses around peak current. Since 2005 the requirements for Class D equipment has been extended to equipment with an input power $P \geq 50W$.

Standard IEC 61000-3-3 is concerned with the limitations of voltage fluctuations and flicker. It is applied to electrical equipment with an input current up to and including 16A per phase and intend to be connected to public low-voltage distribution system [9].

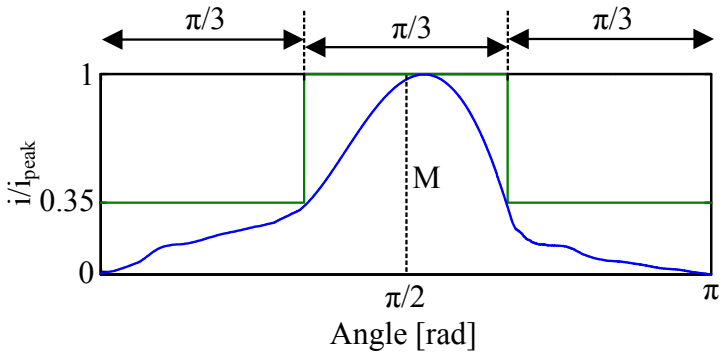


Figure 2.2: *Green - envelop of the input current to define the 'special wave shape and to classify equipment as Class D' [8]; blue - simulated current waveform (overloaded 70 W boost PFC converter with saturated current controller)*

Harmonic order **n**	**Maximum permissible harmonic current** **A**
Odd harmonics	
3	2.30
5	1.14
7	0.77
9	0.40
11	0.33
13	0.21
$15 \leq n \leq 39$	$0.15 \cdot \frac{15}{n}$
Even harmonics	
2	1.08
4	0.43
6	0.30
$8 \leq n \leq 40$	$0.23 \cdot \frac{8}{n}$

Figure 2.3: *Limits for Class A equipment [8]*

Harmonic order **n**	**Maximum permissible harmonic current expressed as a percentage of the input current at the fundamental frequency** %
2	2
3	$30 \cdot PF^*$
5	10
7	7
9	5
$11 \leq n \leq 39$ (odd harmonics only)	3
* *PF* is the circuit power factor	

Figure 2.4: *Limits for Class C equipment [8]*

Harmonic order **n**	**Maximum permissible harmonic current per watt** mA/W	**Maximum permissible harmonic current** **A**
3	3.4	2.3
5	1.9	1.14
7	1.0	0.77
9	0.5	0.40
11	0.35	0.33
$13 \leq n \leq 39$ (odd harmonic only)	$\frac{3.85}{n}$	As in Class A

Figure 2.5: *Limits for Class D equipment [8]*

The EMI (electromagnetic interference) is the amount of radiation emitted by electrical equipment when operating. EMI is caused caused by emissions in the radio spectrum due to rapid voltage or current changes, which not only interfere with radio systems but also can cause other equipment to malfunction. This interference might not be so harmful when it appears in household equipment like radio, television but it could result in severe catastrophes when it appears for example in the control system of the airplanes.

Due to universal presence of the electromagnetic devices and their possible negative effects different agencies have tried to put regulations to minimize the electromagnetic emission levels. The European standard [50] considers two different equipment categories. Class B equipment are residential use equipment with no fix place of use with built-in battery, telecommunication terminals, personal computers and auxiliary connected equipment. These equipment should meet the limits described in Figure 2.7. Class A equipment are industrial equipment and should meet the limits shown in Figure 2.6. These equipment are not restricted in their sale but should be considered that in domestic use they might cause radio interferences. The limitations are set for conducted common mode electromagnetic noise in a frequency bandwidth from 150kHz to 30MHz and are measured in μV units with a line impedance stabilization network (LISN).

Frequency range MHz	Limits dB(μV)	
	Quasi-peak	Average
0.15 to 0.50	79	66
0.50 to 30	73	60

Figure 2.6: *Limits for conducted disturbances at the mains ports of class A equipment [50]*

Frequency range MHz	Limits dB(μV)	
	Quasi-peak	Average
0.15 to 0.50	66 to 56	56 to 46
0.50 to 5	56	46
5 to 30	60	50

Figure 2.7: *Limits for conducted disturbances at the mains ports of class B equipment [50]*

The following two tables present limitations of conducted common mode disturbances for equipment which are connected to telecommunication lines (ex. telephone cables connected to ADSL modems can be affected by the PC supply).

Frequency range	Voltage limits dB(μV)		Current limits dB(μA)	
MHz	Quasi-peak	Average	Quasi-peak	Average
0.15 to 0.50	97 to 87	84 to 74	53 to 43	40 to 30
0.50 to 30	87	74	43	30

Figure 2.8: *Limits for conducted common mode disturbances of class A equipment [50]*

Frequency range	Voltage limits dB(μV)		Current limits dB(μA)	
MHz	Quasi-peak	Average	Quasi-peak	Average
0.15 to 0.50	84 to 74	74 to 64	40 to 30	30 to 20
0.50 to 30	74	64	30	20

Figure 2.9: *Limits for conducted common mode disturbances of class B equipment [50]*

2.2 Power factor correction - terminology

As a result of applying different standards, a new research topic has become very popular in power electronics: Power Factor Correction.

In case of pure sinusoidal waveforms the *Power Factor (PF)* can be defined like in equation 2.1. It is always a value between 0 and 1 [11]:

$$PF = cos\phi = \frac{P}{V_{rms(sin)} \cdot I_{rms(sin)}} \tag{2.1}$$

where P is the average power, $V_{rms(sin)}$ and $I_{rms(sin)}$ are the rms voltage and current. The angle ϕ is the phase angle between the current and voltage. This factor is usually called the *displacement factor*. The unity power factor occurs only for pure resistive loads. In this case the current is in phase, has the same shape and has same harmonic spectrum as the line voltage.

Although the line voltage is assumed to be sinusoidal because the harmonic distortion in most of the cases is quite low, the line current is non-sinusoidal due to the nonlinear loads. Therefore the classical definition of the power factor can not be applied. The power factor equation for general voltage and current waveforms can be written as:

$$PF = \frac{V_{rms} \cdot I_{1,rms} \cdot cos\phi}{V_{rms} \cdot I_{rms}} = \frac{I_{1,rms}}{I_{rms}} \cdot cos\phi = K_d \cdot cos\phi \tag{2.2}$$

The factor K_d is called *distortion factor* and it is the ratio of the current to the fundamental and defines the harmonic content of the current. The power factor is dependent on the shift between the current and voltage (displacement factor) and the harmonic content of the current (distortion factor).

The distortion factor can be defined in function of the *Total Harmonic Distortion (THD)*. The THD is defined as a ratio of the rms value of the current not including the fundamental to the rms fundamental magnitude [10]:

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1} \tag{2.3}$$

The K_d is closely related to the THD:

$$K_d = \frac{1}{\sqrt{1 + THD^2}} \tag{2.4}$$

Even if the displacement factor is close to 1, the PF can be low due to substantial harmonic content. Similarly, in case of low harmonic content can not also be guaranteed high power factor due to eventually low value of the displacement factor.

2.3 Converter topologies

Power converter researchers have developed and are developing different techniques, called *Power Factor Correction (PFC)* techniques to meet the different standards and increase the efficiency of different electrical equipment. The reduced harmonic content of the input line current will increase the power factor at the same time. Different publications summaries in form of a survey the different techniques [11]-[14]. Two major categories can be defined depending on whether active or passive components are involved in current shaping: *passive* [15]-[25] and *active* PFC techniques [26]-[49]. The active PFC techniques can also be differentiated into *low switching frequency* and *high switching frequency* solutions [11].

2.3.1 Passive PFC topologies

The passive solutions are simple, robust, efficient, and the most reliable methods for reducing the undesired harmonics without producing EMI. In spite of their effectiveness they have some disadvantages [11]:

- the filter inductors and capacitors are expensive, heavy and bulky
- it is difficult to design
- have poor dynamic response
- lack of output voltage regulation - the output voltage is dependent on the line voltage and the ripple is increasing with the load.
- fundamental components may show a phase shift decreasing the displacement factor
- some circuits are sensitive to line frequency

The standard single-phase uncontrolled diode rectifier has DC output voltage ripple with a frequency twice the line frequency. Adding a filter capacitor in parallel with the rectifier output reduces the output voltage ripple but increases the harmonic content of the line current. The one of the simplest passive filtering method is to add a series inductor at the AC or DC side of the diode rectifier (Figure 2.10 a.) and b.)). With a single inductor and

without an input capacitor in front of the rectifier the maximum achievable power factor is 0.76 [16]. By adding the input capacitor this value can be increased to 0.9. A design proposed by [15] places the inductor on the DC side and adds also diode in series with the inductor and a parallel capacitor to the diode bridge. With such design the harmonic content of the line current can be manipulated such way that the class of the equipment can be changed from D to A. With power level lower than 300W it is easier to meet the norms of class A [15]. With proper filter design [18], which might include not only inductive, but inductive-capacitive filter after the DC capacitor, sinusoidal input current can be obtained with power factor 0.99. The proposed design ensures continuous current operation of the single phase rectifier but is effective for power levels higher than 1.2 kW in the presence of an L-C DC filter. A minimum filter inductance value is required, which affects the size of the filter compared to other components. In [19], it is proposed a cost effective solution for inductive filters at low power levels (70W-150W), obtaining a load dependent filter with a special core using a sloped air-gap. Different passive filter topologies are discussed in [20] combining one inductor and one or more capacitor obtaining power factor between 0.701-0.983 and THD of 0.164-0.646. In [20] it is shown that by rearranging the circuit and by splitting the power factor corrector capacitors, the DC and even harmonic components of the line current can be eliminated. Thus low cost passive PFC circuits can be built to meet current harmonic regulations.

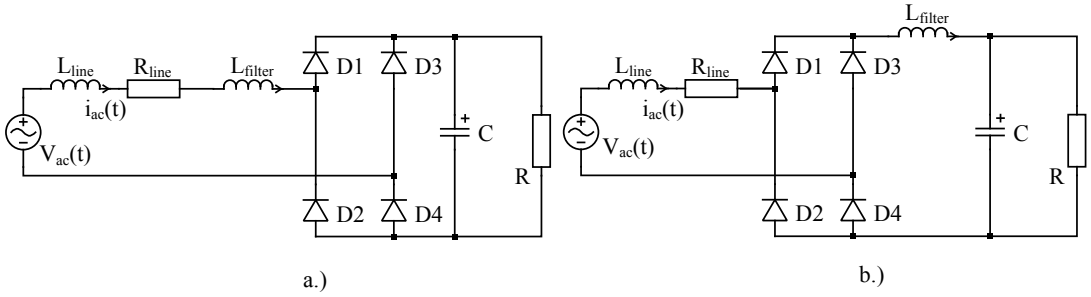


Figure 2.10: *Rectifier with inductor filter [17]*

Introducing a filter capacitor $C_f$to the AC side of the rectifier, may increase the power factor [21]. Beside reducing the line current harmonics the capacitor may be used to improve the displacement factor. The author in [21] also presents how the LC filtered full bridge rectifiers meet the IEC 1000-3-2 standard, class D specifications within 75W-600W power range. In [22] LC filter solutions are discussed for electrical equipment classified according to IEC-1000-3-2 standard and a new, called TLC filter is proposed, resulting in a reduced size of the inductor and the power losses in the magnetic core by 50%.

Designing the filter in such way that it changes the equipment classification according to standard IEC-1000-3-2 form class D to class A is propose by [23]. The advantage is that class A allows larger harmonic content for the input current. It is easier to achieve compliance in class A at lower power level. This change also decreases the size of the inductors, reduces the core costs. However after year 2000 the standard IEC-1000-3-2 requirements for class D equipment have been updated to IEC 61000-3-2, so this technique has lost its applicability.

Resonant passive filter on the AC side of the diode rectifier, proposed by [24] can

eliminate the 3^{rd} harmonic component of the input current obtaining a THD of 0.2 and power factor of 0.97. Improving this topology with a capacitor on the the AC side (Figure 2.11), parallel with the bridge, it can compensate the reactive power [25].

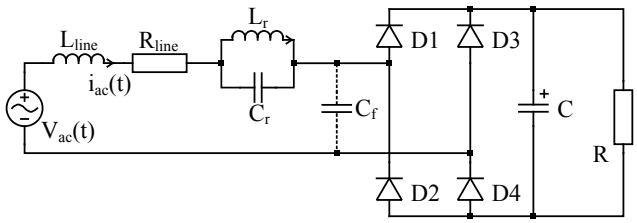


Figure 2.11: *Rectifier with resonant passive filter [25]*

2.3.2 Active PFC topologies

The available instantaneous power of a single phase system is pulsating due to the sinusoidal variation of the voltage. On the other hand switching-mode power supplies draw constant averaged power (Figure 2.12). The excess energy has to be stored in one half period and return it to the circuit in the other half period. The energy can be stored in inductors or capacitors [15]. The passive energy storage devices, like capacitors and inductors are bulky and have big dimensions.

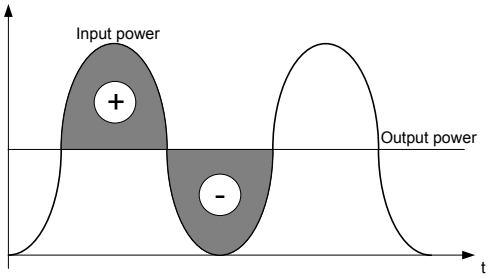


Figure 2.12: *Pulsating input and constant output power*

To reduce the size and weight of the inductors, *active* PFC techniques have been developed. By using high frequency inductors the size of the converter can significantly reduced. If the power conversion increases the costs can also be lowered, compared to the passive solutions.

Some circuits are synchronized to the line frequency. These converters are called *low-frequency PFC* converters. In such circuits the switching losses and EMI are negligible because the switches operate at the fundamental or low-order harmonics of the line frequency. On the other hand they need large magnetic components and the output voltage control is slow [11]. As low-frequency PFC converters does not enjoy great popularity, the majority of the active PFC converters are driven at a frequency much higher than the audible level (which is normally in the 20kHz to few hundred kHz range). These converters are *high-frequency PFC* converters. During this thesis work the focus will be on the high-frequency PFC converters.

Different *single stage* topologies were proposed during the research years [26]-[28]. To provide isolation, regulated output voltage and power factor correction at the same time it requires complex topology designs resulting in expensive magnetic components (coupled inductors, custom made transformers). Single stage power factor converters have a reduced number of switching components and also the number of control loops is reduced [27]. If the requirements allow non-sinusoidal currents single stage PFC converters can meet the demands. If the requirements ask for perfect sinusoidal line current with low harmonic distortion, *two-stage* PFC converters are the most suitable [28]. Most of the industrial products (PC power supplies, security alarm systems, etc.) use two-stage converter for power factor correction with a second stage DC-DC converter to comply with load demands (fast output voltage dynamics in response to load changes). This is the result of the fact that it is relatively easy to make a simple power factor preregulator and simply using some standard (flyback, forward, half or full bridge) converter to isolate the load from the grid.

The *boost* switching cell is very often used as a front-end converter (Figure 2.13) in PFC applications. This is due to the simplicity of the circuits and some natural characteristics like the fact that the inductor current follows the line voltage. It is one of the most popular front-end converters with high efficiency for two-stage PFC converters and most commonly used on the market. Depending on the number of active switches we can talk about one switch, two switch or four switch boost converters [12],[14].

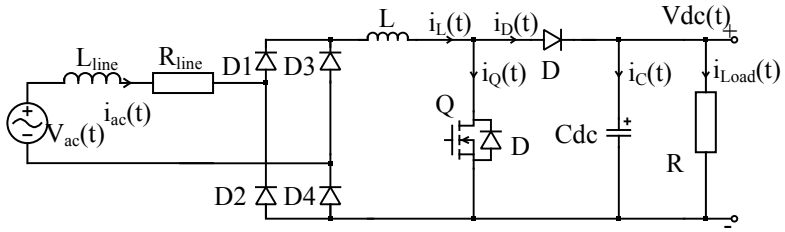


Figure 2.13: *Boost PFC circuit - Basic topology*

Some disadvantages of the boost converter are the lack of a switch between the line and load (no protection against inrush current, over-voltage, overload, short circuit) and higher output voltage than input voltage. Some protection can be obtain by using isolated version of boost converter.

The boost converter can operate in different conduction modes:

Operating in *Discontinuous Conduction Mode - DCM* boost converters are seldom used as stand-alone PFC systems for universal input voltage and only for less than 250W. The difference between the peak and rms values of the current is higher at high power and the switch will have higher current stress [36]. At high power level the current has a rising and a falling edge on the boost inductor and introduces high frequency harmonics. Though there is the advantage of zero current turn-on of the switching device limiting the switching losses and EMI generation to the turn-off sequence [29]. This operation mode does not lead to fully sinusoidal input current, although it follows the line voltage automatically. The control of the converter is simpler because the current control loop can be neglected. On the other hand there is high current stress on the inductor of

the boost cell and voltage stress on the switching components. For a stand alone boost PFC converter some solutions with interleaving techniques are proposed by [31]-[34] to obtain sinusoidal input current with boost converters operating in DCM reducing the total inductor current ripple. This leads to increased size of the converter, the number of switches and the size of passive components. Frequency modulation can improve the sinusoidal shape of the input current but the wide range of the frequency needs more complex filtering and circuit design. A modulation technique, like injecting a second order harmonic component to the reference wave carrier obtaining an amplitude modulation, is proposed by [35]. This method reduces the amplitude of the third current harmonic. The drawback of this method is the synchronization to the line voltage needs additional circuit parts.

Combining DCM-operated boost converters with other DC-DC switching cells to reduce the number of switching devices results in single-stage PFC topologies. Operating on wide input voltage range these converters generally have an internal DC bus voltage variation. This result in high component stress.

Boost switching cells operating in *Continuous Conduction Mode - CCM* are the most used for PFC. It has been shown in [36] that the CCM operated boost PFC converters have lower switching stress on the switching semiconductors compared to the DCM operation, but this is penalized with higher revers recovery time of the boost diode in case of CCM. The boost PFC circuit operating in CCM reduces the current ripple in the inductor, the conduction losses and requires smaller EMI filter but it needs more advanced control strategies to obtain the input current shaping. For wide output voltage range applications another step-down converter is needed cascade with the boost converter (Section 2.3.4). The boost converter is the current shaper and with the additional converter fast output voltage dynamic can be obtained.

Some solutions exist to operate the boost converter on the border of DCM and CCM, also called transition or *Critical Conduction Mode - CRM* [38]. The ON-tome is kept constant but the OFF-time is varying according to the diode current. In this operation mode the revers recovery losses of the diode are eliminated and near zero current switching, so called valley switching is also achieved. Variable on-time control with valley switching and frequency limitations is proposed by [39] and [40] to reduce the input current distortion and the THD. Limitation of this operation mode is the variable switching frequency, which can lead to radio interferences [41] and the high frequency differential-mode harmonic content of the input current makes the input filter design costly [29].

At high line current applications *interleaved PFC boost converters* are used and all of the three operation modes are investigated (*DCM*, *CRM* and *CCM*) (Figure 2.14) [42]-[45]. The advantage of this method is, though the number of magnetic components has increased, the reduced current stress, smaller inductors and MOSFETs with smaller current-rate can be used.

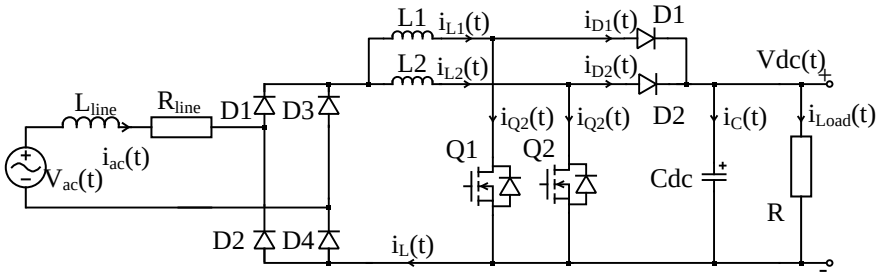


Figure 2.14: *Interleaved boost PFC circuit*

Buck converters as front end or stand-alone PFC converters are seldom used as voltage source converters. The main reason is that at certain input voltage levels, when output voltage is higher than the input voltage the there is no current flow from the input to the output. Thus the line current will not be sinusoidal [12],[46]. Advantage of the buck converter is that it can provide over-current protection due to the switching MOSFET on the main power line, so inrush current is well controlled.

Buck converters are mostly used in current source type PFC circuits. Different control strategies are proposed by [47]-[49], like delta modulation or inductor voltage control. The current source type buck converters can operate for all values of the input voltage, but the output current has to be higher than the instantaneous input current. These type of converters are not so popular, although they can be used in some low-voltage high-current applications like DC motor drives [12].

2.3.3 Electro-magnetic compatibility - EMI filters

In a PFC circuit the main source of the conducted EMI is the switching transistor and the diode. Two kind of electromagnetic conducted noises exist:

Differential mode - DM noise is caused by the normal operation of the converter: the high switching frequency ripple of the current through the boost inductor.

Common mode - CM noise is caused by high frequency voltage ripple in the switching transistor. There is a small capacitance between the transistor and heat sink with an insulation material. Though it is of order of tens of pF the turning OFF and ON the transistor (fast charging and discharging) results in a significant current flow through this parasitic capacitance. A typical AC line connected EMI filter is presented in Figure 2.15. The C_{x1} and C_{x2} capacitors affect DM noises while the two C_y capacitors damp both differential an common mode noises. The L_C common mode choke rejects CM noises. Many applications use only the leakage inductance of the coupled common mode inductors as L_D [51].

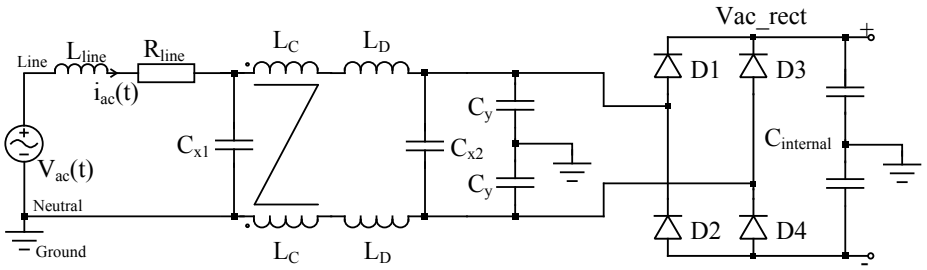


Figure 2.15: *Basic EMI filter topology for line connected power supplies*

The limitations for EMI are presented in EN 55022 standard [50]. This standard contains limitations for conducted noises between 150 kHz and 30 MHz and radiated noises from 30 MHz up to 2 GHz. Several publications that discuss the design problem of the EMI filter [51], [52], [53] and [54] present a possible high frequency model of the boost inductor and the output capacitor to approximate a good impedance characteristics up to 30MHz. After having these models the noise propagation problem in the converter is examined through the DM-loop and CM-loop models. [55] and [56] analytically analyze and predicts the active and passive DM and CM noise sources and also makes the high frequency model of the inductor and capacitor. [57] proposed a filter design method suitable for AC-DC and DC-DC switch mode power supplies. This method requires only the knowledge of the maximum and minimum value of the CM and DM noise impedance amplitude. [58] present a CM filter which reduces the size of the filter inductor. The layout and component placement problem is discussed in [59], [60], [61]

2.3.4 DC-DC converter topologies

For two-stage PFC/DC-DC converters a second converter is connected in series with the first stage current shaper in order to regulate the output DC voltage or current. Depending on the power level and application a step down converter follows the PFC pre-regulator. For an output power range from few W to MW range non-isolated buck or the isolated flyback or buck-derived forward, two-transistor forward, half-bridge or full-bridge converters are generally used. These converters are operated in CCM to reduce current stress and maintain better controllability.

2.3.4.1 Non-isolated switching topologies

- *Buck converter*

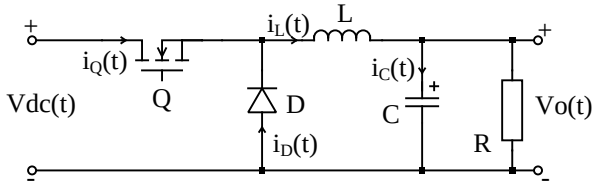


Figure 2.16: *Buck converter - Basic topology*

The buck DC-DC converter (Figure 2.16) can operate either in DCM either CMM. Buck converters operating in DCM are designed for low power applications especially with large output load variation. The buck converter is reliable because the output voltage and current can be easily regulated under fault conditions [62]. To operate the buck converter in CCM two conditions have to be satisfied:

$$\Delta i_L \leq 2I_L \tag{2.5}$$

$$\Delta v_o \leq 2V_o \tag{2.6}$$

where Δi_L is the inductor current ripple and it should be smaller than the average inductor current I_L and the output voltage ripple Δv_o should be smaller than twice the average output voltage V_o. Satisfying these two conditions it can be determined a critical value of the output inductor L_C (2.7). If the inductor $L < L_C$, the converter will operate in DCM. In case of $L > L_C$, the converter operates in CCM [62].

$$L_C = \frac{R \cdot (1 - D)}{2 \cdot f_S} \tag{2.7}$$

It is visible that the critical inductance is directly proportional to the load resistance R and inverse proportional to the switching frequency f_S. By changing these two parameters the critical inductance can be reduced. Advantage of the DCM or CRM operation of the buck converter is the zero-current-switching. On the other hand in DCM the output voltage becomes load dependent and the converter characteristics change and also the components have to be overrated due to high peak currents. For better design and controllability the CCM operation is preferable.

The output voltage of the buck converter is given by:

$$V_o = D \cdot Vdc \tag{2.8}$$

2.3.4.2 Isolated switching converters

In order to prevent the load from the grid disturbances, high voltage and current stresses isolated DC-DC converters are used. Different step-down isolated converters are derived from buck converter. These converters have to operate with high input voltage obtained from the boost PFC converter and reject the two times line frequency voltage ripple.

- *Flyback converter*

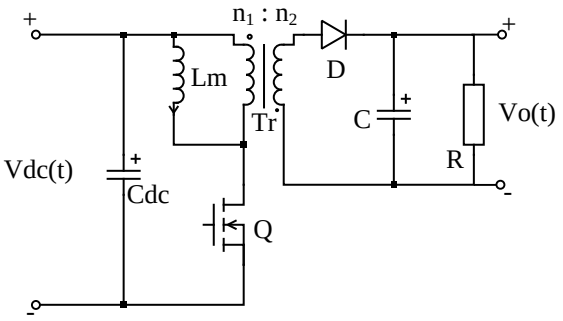


Figure 2.17: *Flyback converter*

The flyback converter (Figure 2.17) is a buck-boost derived isolated converter and due to circuit simplicity it is mostly used for low power low cost applications (no filter inductor needed). The power range is up to 250W and it is used used for laptop power supplies, battery chargers, etc... The transformer of a flyback converter is more like a coupled inductor and the polarity of the windings, unlike at traditional transformers, is reversed to obtain positive output voltage [10]. Its major disadvantage is the high voltage stress on the switching transistor due to ringings caused by the transformer's leakage inductance and the MOSFET's internal capacitance. To overcome this two-switch flyback converter topologies were developed [63]. The output voltage of the flyback transformer is obtained by:

$$V_o = \frac{n_2}{n_1} \cdot \frac{D}{1-D} \cdot Vdc \tag{2.9}$$

where n_1 and n_2 are the number of turns in the primary and secondary windings of the "flyback transformer", D is the duty cycle and Vdc is the input voltage.

Some applications use flyback converters even as PFC converters connecting it to a diode rectifier bridge [64] and achieving high power factor. Disadvantage of it that it has an output voltage ripple with twice the line frequency.

- *Forward converter*

The basic forward converter topology is presented on Figuire 2.18. The main application area is up to 4-500 W power level. It is also a single transistor isolated buck-derived step down converter with grounded MOSFET.

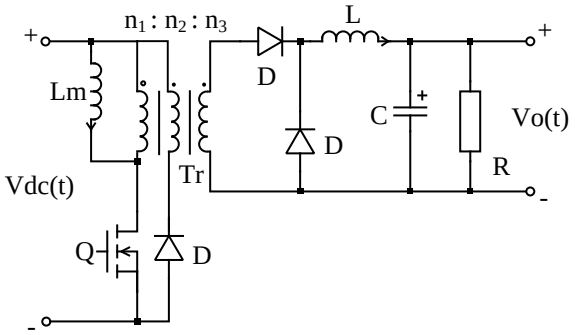


Figure 2.18: *Forward converter - Basic topology*

To demagnetize the forward transformer, a third winding is required which increases the complexity of the transformer and the price of the converter. The number of turns of the demagnetizing winding is usually $n_2 = n_1$. To avoid the transformer saturation hence operate the magnetizing inductance current in discontinuous conduction mode the duty cycle must be limited to 50% of the switching period. Hence the output voltage can be found as:

$$V_o = \frac{n_3}{n_1} \cdot D \cdot Vdc \tag{2.10}$$

To reduce the transformer complexity different other demagnetization methods were developed. Resonant reset forward converter (Figure 2.19 a.)) has only a two winding transformer. It is demagnetized by a resonant circuit which consists of the magnetizing inductance of the transformer and the internal capacitance of the switching MOSFET [65]-[66]. The disadvantage of this method is that the peak value of the drain-source voltage is dependent on the component parameters (magnetizing inductance and internal capacitance of the MOSFET) - Figure 2.19 c.)

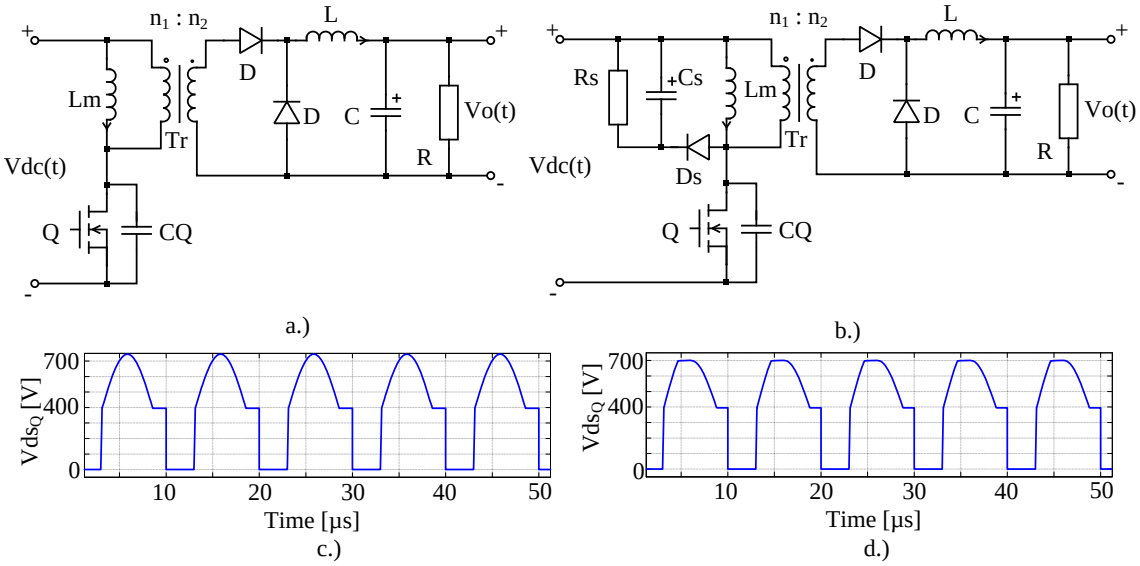


Figure 2.19: *a.) Resonant reset forward converter; c.) Drain-source voltage of the MOSFET in case of resonant reset; b.) RCD clamped forward converter; d.) Drain-source voltage of the MOSFET in case of RCD clamp;*

Another demagnetization technique is introducing an RCD (resistor, capacitor and diode) snubber parallel with the primary winding of the transformer (Figure 2.19 b.)). The capacitor charges to the voltage level of the diode to reset the primary winding of the transformer, when after the resistor dissipates the energy accumulated in the capacitor. With this the voltage stress on the switching MOSFET can be reduced below $2 \cdot Vdc$ (2.19 d.)). The peak level of the drain-source voltage can be adjusted by choosing the right R and C components [67]. Disadvantage of this method is the resistor dissipates energy thus there is a decrease in efficiency.

Synchronous rectification is introduced on the secondary side of the forward transformer in order to increase efficiency as MOSFETs have much lower ON-resistance than

the diode bridge [67]-[69].

- *Two switch forward converter*

Many analysis on two switch forward converter, shown in Figure 2.20, were presented for low to medium power level applications [70]-[71]. The two MOSFETs are driven by the same gate signal [10] but a floating gate driver is needed for the upper transistor. The major advantage of it is that the switching components have to withstand only once the input voltage. The magnetizing energy from the transformer is returned to the DC link capacitor through the two primary diodes. The demagnetizing winding is also removed compared to the basic forward topology.

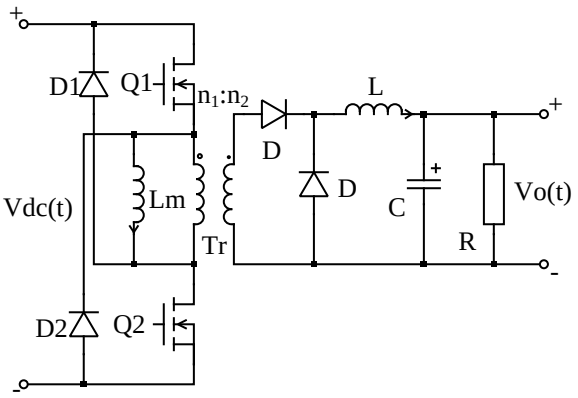


Figure 2.20: *Forward converter - Basic topology*

- *Full bridge converter*

Generally the full-bridge converters (Figure 2.21) are used in a power range of 500W and above.

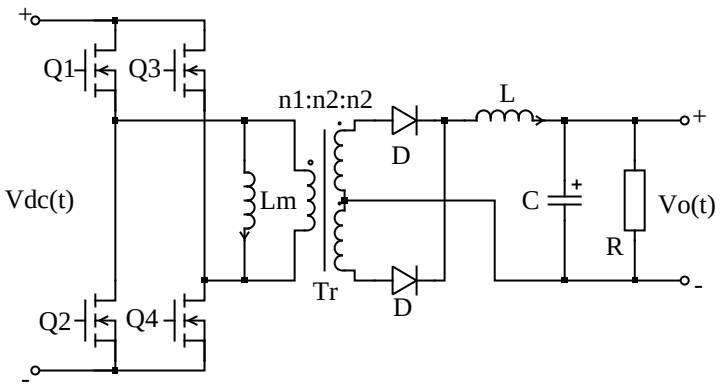


Figure 2.21: *Full-bridge converter - Basic topology*

It is not recommended at low power level due to high number of components. Another disadvantage is that floating gate drivers are needed for the upper transistors. The two upper MOSFETs are turned on alternately with the two lower ones during the on time.

The dead time has to be determined carefully to avoid undesired short circuits. The basic topology uses transformer with center-tapped or double secondary winding.

The output voltage is given by [10]:

$$V_o = \frac{n_2}{n_1} \cdot D \cdot Vdc \tag{2.11}$$

- *Half bridge converter*

The half bridge converter (Figure 2.22) is operated mostly up to 1 kW. It is similar to the full bridge converter in operation. The only difference is that the second leg is replaced with large-value capacitors $C1$ and $C2$. Due to these capacitors the MOSFETs have to withstand a voltage stress of only the supply voltage level.

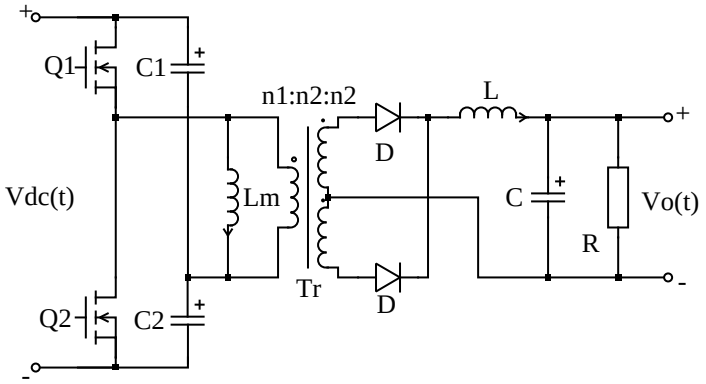


Figure 2.22: *Half-bridge converter - Basic topology*

The output voltage is given by [10]:

$$V_o = 0.5 \cdot \frac{n_2}{n_1} \cdot D \cdot Vdc \tag{2.12}$$

- *Phase-shifted full-bridge converter*

The phase-shifted full-bridge DC-DC converter (Figure 2.23) is a very commonly chosen solution in medium-high power range applications. The presented circuit is a special case, including synchronous rectification to improve efficiency and current double to meet the load demands for high current [72]. Basic operation of the converter was described in many publications [73]-[78]. The leakage or some additional inductance is used together with the parasitic capacitances of the switching MOSFETS to realize the zero-voltage-switching (ZVS).The full bridge MOSFETs are switched with fixed duty cycle (50%) but the switching wave of the second leg is shifted. The overlap between the the two switching signals is determined by the control algorithm.

The output voltage can be calculated based on:

$$V_o = \frac{n_2}{n_1} \cdot D_{eff} \cdot Vdc \tag{2.13}$$

where D_{eff} is the duty cycle on the transformer, determined by the phase shift.

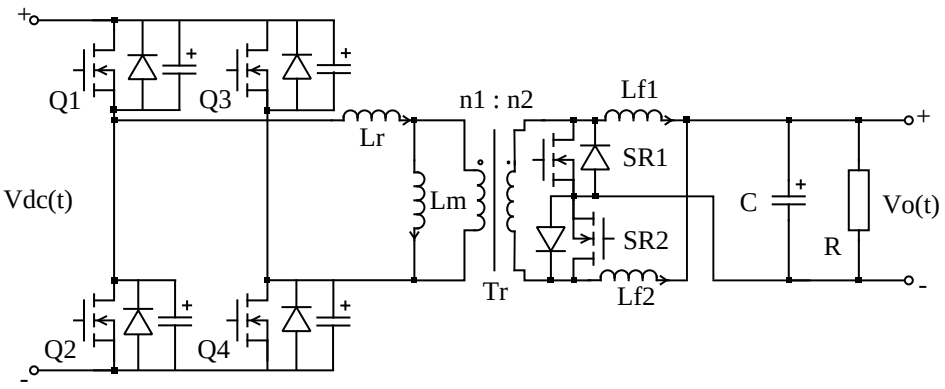


Figure 2.23: *Phase-shifted full-bridge converter with current doubler*

2.4 Analog and digital controllers on the market

As digital control needs to be competitive with analog control in efficiency and price a list of available analog controller ICs were investigated as follows:

Comp code	Manufact.	Control method	Min. price (DKK)	Max. Price (DKK)	Comments
UC2853 8 PINS	TI/Unitrode	- Average current mode	12.89	37.63	- 75 kHz switching frequency
UC2854 16 PINS	TI/Unitrode	- Average current mode	17.14	28.18	- above 200kHz switching frequency - wide input voltage range - wide line frequency range
UCC28019 8 PINS	TI	- CCM	5.62	11.16	- 65 kHz switching frequency - 100W to >2kW range converter
UCCx817/ 18 16 PINS	TI	- Average current mode	12.34	13.56	- BiCMOS technology - 100 kHz switching frequency
UCC2851x 20 PINS	TI	- Average current mode - CCM		19.32	- PFC/PWM Combo - PFC switched at the same frequency with PWM - PWM switched with double of the PFC frequency
UCCx805x 8 PINS	TI	- CRM	6.88 *	10.63 *	- Sensing the switch current

Comp code	Manufact.	Control method	Min. price (DKK)	Max. Price (DKK)	Comments
FAN4803 8 PINS	Fairchild	- Average current mode - CCM	14.44	27.02	- Low startup current - Combo PFC/PWM - Load power limited by PWM stage
FAN4810 16 PINS	Fairchild	- Average current mode - CCM	7.94	15.59	- 76kHz Switching freq.
FAN4822 14-16 PINS	Fairchild	- Average current mode - CCM	18.28	33.49	- High power application - Zero voltage switch
FAN7528-30 8 PINS	Fairchild	- Voltage mode control - CRM	5.49	11.61	- No line voltage sensing
ML4802 8 PINS	Fairchild	- CCM - Average current mode			- Combo PFC/PWM - Leading edge PFC - Trailing edge PWM
ML4812 16 PINS	Fairchild	- Peak current mode		9.89	- Programmable ramp compensation -> when D>50% and working in CCM - 98kHz switching freq.
ML4821 18-20 PINS	Fairchild	- Average current mode	29.61	46.37	
IR1150S 8 PINS	International Rectifier	- One cycle control - CCM		21.26	- No line voltage sensing - Programmable switching frequency - Soft start
L6561-62 8 PINS	STMicroelectronics	- CRM	4.91	14.42	- Low consumption - Up to 300W
LT1248 16 PINS	Linear Technology	- CCM/DCM	48.76	64.28	- Flexible switching frequency - Universal input - Up to 1500W
LT1249 8 PINS	Linear Technology	- CCM/DCM		79.03	- 100kHz switching frequency - Up to 1500W
MC33368 16 PINS	ON Semiconductors	- CRM	10.34	17.09	- Low power high density power supplies
MC33262 MC34262 8 PINS	ON Semiconductors	- CRM	3.67	7.01	- High efficiency - Current-mode PFC
NCP1653 8 PINS	ON Semiconductors	- Peak or average current mode - CCM	7.34 *	11.14 *	- 67 or 100 kHz switching frequency

Figure 2.24: *The PFC controller ICs available on the market*

All the prices are based on www.farnell.com database.

Prices with * are based on www.rsonline.dk database.

Before designing digital control the proper digital controller has to be chosen. There are many digital controllers with fixed or floating point Arithmetical-Logical-Unit (ALU), 16 or 32 bit word structure, different calculation speed and at last but not at least the cost of the processor has to be also taken into account. The type, speed, characteristics, number of I/O channels, etc..., all have major influence on the controller design. In the followings a brief market survey will be presented on digital signal processors, controllers and microcontrollers. All the prices and data are presented based on www.farnell.com database.

- Microcontrollers

	ATMEL	
Family	ATXMEGAx	AT32UCx/AT91SAM7x
Word structure	16 bit	32 bit
CPU speed	32 MHz	50-150 MHz
Memory	16-32 kB	16-256 kB
Dedicated PWM	Timer/Compare module	yes
Price	min: 24/max: 33 DKK	min: 28/max: 40 DKK

- Digital signal controllers

	Freescale Semiconductors	
Family	MC9S12x	MCF51x/MCF52x/DSP56F8x
Word structure	16 bit	32 bit
CPU speed	32-80 MHz	50 MHz
ALU	fixed point	fixed point
Memory	12-128 kB	32-256 kB
Dedicated PWM	yes	yes
Price	min: 22/max: 37 DKK	min: 26/max: 47 DKK

	Microchip			TI
Family	dsPIC30fx	dsPIC33fx	PIC32MXx	C2000
Word structure	16 bit	16 bit	32 bit	32 bit
ALU	fixed point	fixed point	fixed point	fixed point
CPU speed	15-40 MHz	40 MHz	40-80 MHz	20-150 MHz
Memory	6-144 kB	6-256 kB	8-128 kB	16-512 kB
Dedicated PWM	yes	yes	yes	yes
Price	min: 17 DKK max: 28 DKK	min: 19 DKK max: 20 DKK	min: 20 DKK max: 32 DKK	min: 40 DKK max: 61 DKK

- Digital signal processors

	Analog devices		TI	
Family	ADSP-BF5x	ADSP-21xx	C2/5/6000	C6000
Word structure	16/32 bit	16/32 bit	16/32/64 bit	16/32/64 bit
ALU	fixed point	floating point	fixed point	floating point
CPU speed	20-533 MHz	28-400 MHz	20-1000 MHz	57-300 MHz
Memory	16-128 kB	16-256 kB	16-128 kB	1 MB
Dedicated PWM	yes	yes	yes	yes
Price	min: 74 DKK	min: 212 DKK	min: 35 DKK	min: 59 DKK
	max: 92 DKK	max: 242 DKK	max: 52 DKK	max: 86 DKK

All the prices are from www.farnell.com database. The minimum price is the unity price when purchasing a minimum number of 100 components while the maximum price is the buy-one price.

From the above survey the economic reasons for using digital control is not so clear. On the other hand, with falling prices of microcontrollers and increasing demands on the performance of power converters introducing digital control seems to be a reasonable option for the future development of power converters. The opportunity to realize non-linear, predictive and adaptive control strategies and monitoring the system behavior provides a strong reason why digital control could yield worthwhile advantages compared with state-of-art analog controllers. From the above list a UCC28512 combo PFC/PWM analog and two digital controllers, a dsPIC30F1010 and a dsPIC33FJ32GS406, were chosen for further investigations. To embed the Microchip microprocessors to the power board, the corresponding pins have to be connected to an RJ11 connector and through USB and ICD2/3 In-Circuit Debugger device the microprocessors can easily programmed. The firmware developing environment is Microchip Mplab.

2.5 Control strategies

The structure of the PFC and DC-DC converter control usually consist of two loops: one fast current control and a voltage control loop with lower dynamics. Different control techniques exist to shape the current and at the same time control the output DC voltage:

- *Peak current control*

  In standard peak current control the switching or inductor current peak is sensed and compared to a reference current value. Additional external ramp compensation is needed. In PFC applications this leads to input current distortion around voltage zero-crossing. While the current peak current follows the programmed sine wave the average current might not follow it and this might cause input current distortion [82].

- *Valley current control*

  In standard valley current control the inductor current valley is sensed and compared to a reference current value.

- *Average current control*

Average current control is the most used control method nowadays. Instead of controlling the peak current, the average inductor current is controlled increasing with this the current noise immunity [82].

- *Nonlinear carrier control*

  The nonlinear carrier control method is based on the comparison of a voltage which is proportional to the switching current and a parabolic carrier waveform, generated from the feedback voltage signal [83]. This technique leads to a nonlinear approach of the PFC converters. In recent publications [84] nonlinear analysis of the PFC converters are highlighted. It is a simpler controller than average current control but also much sensitive for instability.

Due to cost reasons the majority of the control algorithms are implemented as analog circuits. Several analog chips have been developed for different control methods like average current control, peak current control, nonlinear carrier control, hysteresis control etc. With the growth of the digital techniques and the advent of low cost and high speed *Digital Signal Processors (DSP)* with embedded control peripherals (pulse width modulation (PWM) generator, analog-digital converter) more complicated control algorithms can be developed and implemented in these digital controllers. This tendency is visible in the latest researches in control of PFC converters [85]-[96].

In analog current control the inductor or switching current is monitored continuously and the switching pulses are generated from comparison of the measured and a reference current and the switching frequency is in the tens of kHz up to MHz range. The implementation in DSPs of the same control algorithm as it is in the analog controllers meets some difficulties. Fast *analog-to-digital converters (ADC)* and large signal processing capability are needed because sampling and processing delay can influence the control efficiency. The latest DSPs with increased speed, increased processing capability and low cost with adequate controller design can overcome these limitations in controller design.

The control of the system can be done with the methods of the traditional control theory and controller design only if a restrictive assumption of the system is considered. By linearizing the real-world system and designing linear controllers one will put constrains and limitations for operating space. Though standard digital linear current regulation based on the small-signal model of the converter, presented by [86],[87] has good transient response. The reference current amplitude is defined with only a voltage compensator.

Many control problems involve uncertainties in the model parameters. This may be due to a slow time variation of the parameters due to aging, temperature, mechanical shock. To overcome these limitations different nonlinear control strategies were developed which can be implemented in digital controllers:

- Hysteresis control

  It was firstly introduced in SMPS control by [102]. For the controlled variable two margins are determined, within this band (dead band) no control action is taken, but when reaching the limits - usually the switching boundaries - the control decisions are taken. Disadvantage of it is the variable switching frequency.

- Model-reference adaptive controller

It is assumed that the system structure is known but the parameters are unknown. A reference model of the system is designed with the desired output. This measured output is compared to the model output and a feedback adaptive law is updating the controller parameters [104].

- Self-tuning controller

  The controller is coupled with an on-line parameter estimator [105]. Such way the the controller parameters can be adjusted to the variable system parameters.

- Fuzzy controller

  Fuzzy controllers combine the human's heuristic knowledge with the conventional control engineering [101].

A possible solution to improve digital control algorithms is predictive technique [88],[89]: the duty cycle for the next switching sequence is calculated based on the present input and output sensed values to minimize or cancel the error of the controlled variable. [88] proposes different modulation techniques for different current control methods: trailing edge modulation for valley current control, leading edge modulation for peak current control and triangle (dual edge) modulation for average current control. [89] introduces an input voltage feed forward component in the predictive algorithm to compensate the calculated duty cycle against the input voltage variations and stabilize the output voltage. As the duty cycles are calculated in advanced, the speed of the DSP is not a critical factor and near unity power factor at high switching frequency can be achieved with low cost DSPs.

If the sampling frequency is too high, after the sampling process there will be not enough time for calculations. If it is too low it introduces aliases. A sampling frequency equal to the switching frequency is proposed by [90]. The sampling instance can be performed or at the middle of the on-time or at the middle of the OFF-time of the MOSFETs. It depends on the duty ratio. New alternating edge sampling is proposed which guarantees the switching noise immunity. [91] proposes a sampling algorithm with variable sampling point for fix frequency hysteresis controllers.

Some solutions exist for implementing digital control algorithms on a *Field Programmable Gate Array - FPGA*. [92] proposes an input voltage sensorless DPFC with $\Sigma\Delta$ dithering and resulting in low resolution PWM. In order to reduce the calculation time and increase the switching frequency a duty-cycle parallel control is proposed by [93] with reduced number of gates. Results show that unity power factor can be achieved in transient and steady state operation mode. A robust and good transient response controller is presented in [94], [95]. This algorithm is using Fuzzy logic and with its membership functions based on the inductor current error and output voltage errors it makes the control decisions. The price of FPGAs is relatively high, depending on the number of gates inside, (from 63 DKK - www.farnell.com) so it does not result in cost effective controller design.

Duty-ratio feed-forward is proposed by [96] in order to keep resistive the input impedance of the converter and keep low current THD. This method eliminates the non-unity power factor present at voltage zero-crossings.

As the second stage converter is also a high frequency DC-DC converter, similar current and voltage control techniques can be applied to regulate the output voltage and current.

From the above listed control strategies the linear PI controller and the nonlinear fuzzy controller will be selected for further investigation.

2.6 Summary

The chapter started with a brief description of the standards which limit the current harmonics and voltage disturbances impressed by the low-voltage line connected devices. After the power factor calculation terminology different power factor corrector techniques and DC-DC converter topologies for different power levels were presented.

In power factor correction techniques major focus was on active solutions and within this the boost-type converters. Their operation modes were discussed in details. Advantage of the boost converter in power factor correction is that it is simple and by construction it ideal for current shaping. Disadvantage is the lack of switch on the main current path and the high output voltage. Interleaving techniques are used for boost converters at high power levels to reduce the current stress on the switching devices and the size of the boost inductor. Disadvantage is the increased number of magnetic and switching components. To obtained the output required output voltage a second stage DC-DC converter is required.

Different DC-DC converter topologies exist according to the required power level. Isolated topologies were mainly discussed so this way galvanic isolation between the load and the line is obtained. Brief presentation of the EMI filter and filter design was made.

Brief survey is presented on the available analog and digital controllers on the market and also the analog and digital controllers used in later design were defined

Different control solution were also discussed making emphasis on their programmability in digital signal processors. The most common controller type in the presented control strategies is the PI controller. Also the possibility of using nonlinear control solutions in digital control, like fuzzy controller, is discussed. The two above controllers will be discussed in details in the following chapters.

Considering the two applications presented in the work motivation, two sets of PFC and DC-DC converters were chosen for further investigation. At low power level (SECURITAC) simple boost will serve as current shaper while an RCD clamped forward converter will deliver the required output voltage. For middle power range (INLED) an interleaved boost PFC converter will be designed while due to high output current demands a phase-shifted full-bridge converter with synchronous rectification and current doubler will be investigated, built and controlled. As visible, interleaving technique is present in both middle power topologies. This will increase efficiency by reducing the current stress and the size of the magnetics but at the same time will increase the number of components thus the overall cost.

Chapter 3

Digital control for switched-mode power supplies

Digital controller design requires accurate knowledge about the power converter. The following chapter will present the small signal modeling of the different converter topologies selected in Chapter 2, designing digital controllers based on the discretized transfer functions. The two controller types mentioned earlier (PI and Fuzzy) and used in later digital implementation are discussed at the end of the chapter.

Different control strategies exist for SMPS applications. In the present the state-of-art analog controller are dominating the control of such applications. As shown in Figure 3.1 some control solutions can not be done with digital controller (peak current control) unless using very high sampling frequency or analog comparator of the microcontroller. Most of the control strategies used in analog controllers can be implemented in digital ones (average current control, hysteresis control). With the emerging of the digital controllers new control strategies like adaptive, predictive, fuzzy control used in different other industry areas can be optimized for high frequency power supplies.

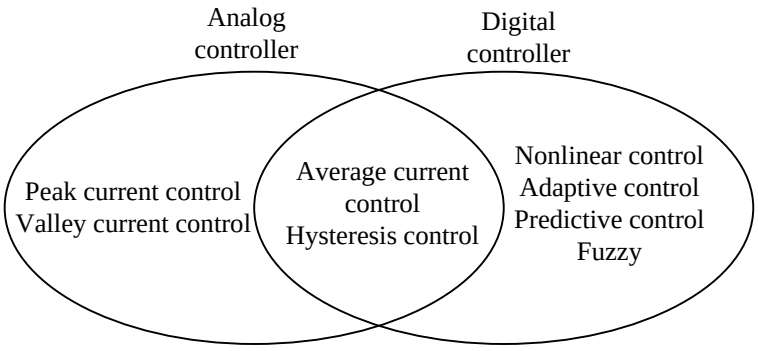


Figure 3.1: *Analog controller vs. digital controller*

In the following sections the challenges in digital control will be presented followed by the analytical modeling of the converters for linear control and introduction of the nonlinear fuzzy controller.

3.1 Challenges in digital control

When implementing digital control, the continuous analog signals are transformed into digital values through the analog-to-digital converters. The digital controller output is then converted back to continuous signals through the PWM modules in form of duty cycle. These two processes introduce undesired noises and disturbances in the system and might produced unwanted oscillations. To avoid these unwanted errors high resolution ADC and PWM and sampling error compensation are used.

The sample-and-hold, the non-zero calculation time and the condition, that the PWM register can not be updated instantaneously, introduces delay in the digital control system. The result is phase margin reduction. To stabilize the system this delay has to be included in the controller design, described later in Section 3.2.4 and 3.3.

To avoid aliasing effect the sampling frequency of different measured signals has to be determined properly. The current loop will have high bandwidth thus high sampling frequency will be applied to react on fast current changes. As the voltage loop has much lower bandwidth, the output voltage is sampled with much lower frequency. All the sampling issues are discussed in Section 3.2.4.

When determining the control algorithm, the structure of the arithmetical logical unit (ALU) has to be taken into consideration. For advanced control structures (adaptive, predictive, nonlinear control) floating point DSPs have better calculation power while the fixed point microcontrollers can handle simple basic control algorithms (PI controller). Use of fixed-point arithmetics in fixed point microcontrollers makes calculations easier but less flexible and more time consuming than in case of floating point processors. The price of the fixed point microcontroller is much smaller compared to the floating point ones. In the following high frequency converter design and control 16 bit fixed point dsPICs will be used as reference due to simplicity in embedding to the power board and cost issues.

3.2 Modeling the chosen converters

To get the sufficient knowledge of the converter properties and its behavior different types of analysis have to be carried out. Based on analytical calculation a large signal model can be built in different software environments like PLECS or different SPICE programs to get a basic idea of the different voltage and current waveforms. To design a controller with the classical tools of the linear control theory a small signal model of the converter is needed to analyze the system dynamics, to get a knowledge about the system response to different perturbations of the input and output signals. Regarding the earlier presented applications the small signal analysis of the simple boost, interleaved boost and PSFB converters will be presented in the followings.

3.2.1 Modeling of the simple boost converter

3.2.1.1 Average small signal model

It is assumed that the converter is operating in continuous conduction mode. This means that from the large signal model of the converter two switching states can be defined.

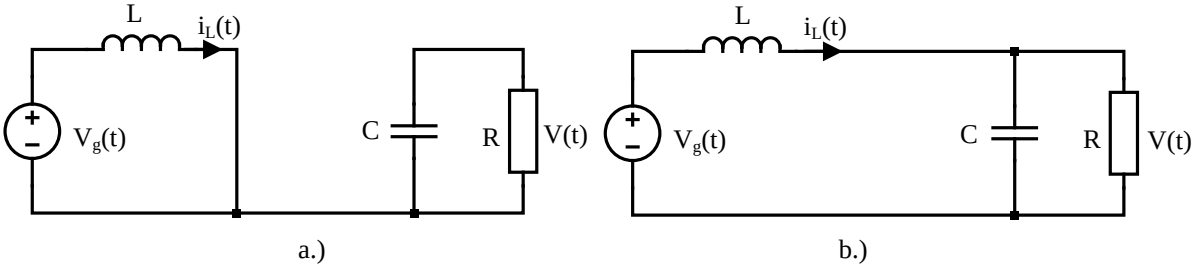


Figure 3.2: *Switching states*

In the first switching state, when the switching MOSFET is ON (Figure 3.2 a.)) the inductor's voltage drop is equal to the input voltage, while the power to the load is delivered from the boost capacitor.

$$v_L(t) = L \cdot \frac{di_L(t)}{dt} = v_g(t) \tag{3.1}$$

$$i_C(t) = C \cdot \frac{dv(t)}{dt} = -\frac{v(t)}{R} \tag{3.2}$$

When the MOSFET is OFF (Figure 3.2 b.)) the current flows from the input through the inductor and boost diode to the load and charging the output boost capacitor. The equations for the inductor voltage and capacitor charging current:

$$v_L(t) = L \cdot \frac{di_L(t)}{dt} = v_g(t) - v(t) \tag{3.3}$$

$$i_C(t) = C \cdot \frac{dv(t)}{dt} = i_L(t) - \frac{v(t)}{R} \tag{3.4}$$

Let us define $\langle v_L(t) \rangle_{T_s}$ and $\langle i_C(t) \rangle_{T_s}$ the low frequency average values of the inductor voltage and capacitor charging current over one switching period. Hence equations 3.1-3.4 become:

$$v_L(t) = L \cdot \frac{di_L(t)}{dt} \approx \langle v_g(t) \rangle_{T_s} \tag{3.5}$$

$$i_C(t) = C \cdot \frac{dv(t)}{dt} \approx -\frac{\langle v(t) \rangle_{T_s}}{R} \tag{3.6}$$

$$v_L(t) = L \cdot \frac{di_L(t)}{dt} \approx \langle v_g(t) \rangle_{T_s} - \langle v(t) \rangle_{T_s} \tag{3.7}$$

$$i_C(t) = C \cdot \frac{dv(t)}{dt} \approx \langle i_L(t) \rangle_{T_s} - \frac{\langle v(t) \rangle_{T_s}}{R} \tag{3.8}$$

According to the the principles of inductor voltage second balance and capacitor charge current balance the inductor voltage and the capacitor current can be defined for the whole

switching period as:

$$\langle v_L(t)\rangle_{T_s} = d(t)\cdot\left(\langle v_g(t)\rangle_{T_s}\right) + d'(t)\cdot\left(\langle v_g(t)\rangle_{T_s} - \langle v(t)\rangle_{T_s}\right) \tag{3.9}$$

$$\langle i_C(t)\rangle_{T_s} = d(t)\cdot\left(-\frac{\langle v(t)\rangle_{T_s}}{R}\right) + d'(t)\cdot\left(\langle i_L(t)\rangle_{T_s} - \frac{\langle v(t)\rangle_{T_s}}{R}\right) \tag{3.10}$$

where $d(t)$ is the duty cycle of the transistor and $d'(t)$ is equal $1 - d(t)$, all values expressed in percentage of the switching period, T_s.

Simplifying equations 3.9 and 3.10 one will get:

$$L\cdot\frac{d\langle i_L(t)\rangle_{T_s}}{dt} = \langle v_g(t)\rangle_{T_s} - d'(t)\cdot\langle v(t)\rangle_{T_s} \tag{3.11}$$

$$C\cdot\frac{d\langle v(t)\rangle_{T_s}}{dt} = d'(t)\cdot\langle i_L(t)\rangle_{T_s} - \frac{\langle v(t)\rangle_{T_s}}{R} \tag{3.12}$$

The last two equations contain only low frequency components.

3.2.1.2 Model linearizing

The power converters have highly nonlinear characteristics. To analyze the system behavior with the methods and tools of the conventional control theory a linear model has to be developed. The model describes the converter only around a specific operating point. To determine the linearized model the differential boost inductor voltage and output capacitor current equations are used.

The above obtained equations are nonlinear. To get Laplace transform of equations or use other frequency-domain methods for making the ac circuit analysis, linear equations are needed.

If the converter is running in steady-state operation mode, the average current and voltage values are equal to the DC values (V_g - input voltage, I_L - boost inductor current, V - output voltage, D - duty cycle ($0 \le D \le 1$) and $D' = 1 - D$). To perform the small signal analysis, a perturbation, a small ac variation has to be introduced in the system. The perturbed average values will look like:

$$\langle i_L(t)\rangle_{T_s} = I_L + \hat{i}_L(t) \tag{3.13}$$

$$\langle v(t)\rangle_{T_s} = V + \hat{v}(t) \tag{3.14}$$

$$\langle v_g(t)\rangle_{T_s} = V_g + \hat{v}_g(t) \tag{3.15}$$

$$\langle d(t)\rangle_{T_s} = D + \hat{d}(t) \tag{3.16}$$

$$\langle d'(t)\rangle_{T_s} = 1 - D - \hat{d}(t) = D' - \hat{d}(t) \tag{3.17}$$

where $\hat{v_g}(t)$, $\hat{i_L}(t)$, $\hat{v}(t)$ and $\hat{d}(t)$ are small ac variations from the average values. Substituting equations 3.13-3.17 in equations 3.11 and 3.12:

$$L \cdot \frac{d(I_L + \hat{i}_L(t))}{dt} = V_g + \hat{v}_g(t) - (D' - \hat{d}(t)) \cdot (V + \hat{v}(t)) \tag{3.18}$$

$$L \cdot \left(\frac{dI_L}{dt} + \frac{\hat{i}_L(t)}{dt} \right) = V_g + \hat{v}_g(t) - D' \cdot V + \hat{d}(t) \cdot V - D' \cdot \hat{v}(t) + \hat{d}(t) \cdot \hat{v}(t) \tag{3.19}$$

$$L \cdot 0 + L \cdot \frac{\hat{i}_L(t)}{dt} = \underbrace{V_g - D' \cdot V}_{DC} + \underbrace{\hat{v}_g(t) + \hat{d}(t) \cdot V - D' \cdot \hat{v}(t)}_{1^{st} order} + \underbrace{\hat{d}(t) \cdot \hat{v}(t)}_{2^{nd} order} \tag{3.20}$$

Neglecting the constant DC and second order components, the linearized inductor voltage balance equation can be written:

$$L \cdot \frac{d\hat{i}_L(t)}{dt} = \hat{v}_g(t) + \hat{d}(t) \cdot V - D' \cdot \hat{v}(t) \tag{3.21}$$

The same manipulation is performed on the capacitor current equation (3.22).

$$C \cdot \frac{d(V + \hat{v}(t))}{dt} = (D' - \hat{d}(t)) \cdot (I_L + \hat{i}_L(t)) - \frac{V + \hat{v}(t)}{R} \tag{3.22}$$

$$C \cdot \left(\frac{dV}{dt} + \frac{d\hat{v}(t)}{dt} \right) = D' \cdot I_L - \hat{d}(t) \cdot I_L + D' \cdot \hat{i}_L(t) - \hat{d}(t) \cdot \hat{i}_L(t) - \frac{V}{R} - \frac{\hat{v}(t)}{R} \tag{3.23}$$

$$C \cdot 0 + C \cdot \frac{d\hat{v}(t)}{dt} = \underbrace{D' \cdot I_L - \frac{V}{R}}_{DC} + \underbrace{D' \cdot \hat{i}_L(t) - \hat{d}(t) \cdot I_L - \frac{\hat{v}(t)}{R}}_{1^{st} order} - \underbrace{\hat{d}(t) \cdot \hat{i}_L(t)}_{2^{nd} order} \tag{3.24}$$

Neglecting the constant DC and second order components, the linearized capacitor current balance equation can be written:

$$C \cdot \frac{d\hat{v}(t)}{dt} = D' \cdot \hat{i}_L(t) - \hat{d}(t) \cdot I_L - \frac{\hat{v}(t)}{R} \tag{3.25}$$

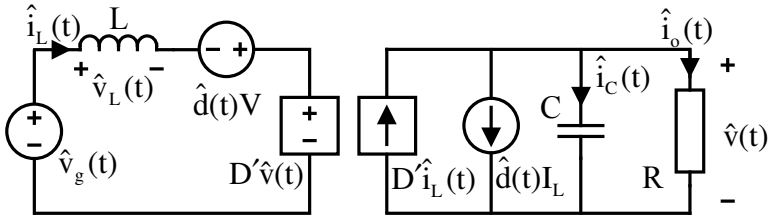


Figure 3.3: *Small signal model of a boost converter*

As the above equations show that the converter can be modeled with DC transformer, dependent and independent current and voltage sources (Figure 3.3). From the above linear equations the required duty cycle-to-output voltage and duty cycle-to-inductor current transfer functions can be determined as following.

3.2.1.3 Converter transfer functions

Having obtained the linearized model the analysis of the converter behavior can be performed with the tools of the conventional control theory. A method to analyze the system dynamics is to use frequency-domain model in form of transfer functions. The transfer of the linearized converter model from time domain to frequency domain is made by taking the *Laplace* transform of the differential inductor voltage and capacitor current equations.

$$L \cdot s \cdot \hat{i}_L(t) = \hat{v}_g(s) + \hat{d}(s) \cdot V - D' \cdot \hat{v}(s) \tag{3.26}$$

$$C \cdot s \cdot \hat{v}(s) = D' \cdot \hat{i}_L(s) - \hat{d}(s) \cdot I_L - \frac{\hat{v}(s)}{R} \tag{3.27}$$

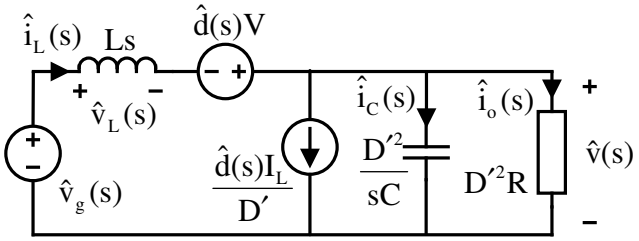


Figure 3.4: *Small signal model of a boost converter in frequency domain*

$$
\begin{aligned}
&\text{a.)}\ M(D) = \frac{1}{1-D} = \frac{1}{D'} \\
&\text{b.)}\ V = M(D) \cdot V_g = \frac{V_g}{D'} \\
&\text{c.)}\ I_o + I_C = \frac{I_L}{M(D)} = D' \cdot I_L
\end{aligned}
\tag{3.28}
$$

By obtaining the Laplace transform of the converter equations and transferring all the values to the left side of the DC transformer (3.28) the required transfer functions can be determined (Figure 3.4).

The dynamic behavior of converter output voltage, $\hat{v}(s)$, is dependent on the input voltage, $\hat{v}_g(s)$, and duty cycle, $\hat{d}(s)$ variations. $G_{vg}(s)$ and $G_{vd}(s)$ are the transfer functions to be determined.

$$
\hat{v}(s) = G_{vg}(s) \cdot \hat{v}_g(s) + G_{vd}(s) \cdot \hat{d}(s) \tag{3.29}
$$

From control point of view the effect of the duty cycle change on the controlled values (inductor current and output voltage) is more important than the effect of the input voltage variation. Thus in the future this last term will be neglected.

The effect of the duty cycle variations on the output voltage can be analyzed through the $G_{vd}(s)$ transfer function. In this case $\hat{v}_g(s)$ is considered equal to zero. From the ac equivalent circuit using the Kirchhoff's voltage law, the equations are presented in the followings.

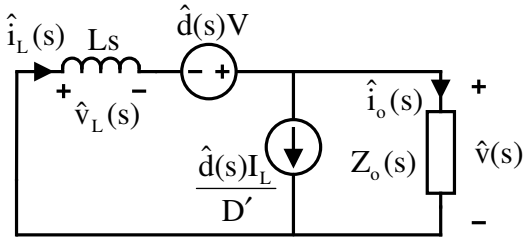


Figure 3.5: *Circuit describing the effect of $\hat{d}$ on $\hat{v}$*

Considering that there is a $\hat{d}(s)$ dependent voltage source and a current source in the ac small signal model (Figure 3.5), the superposition of the terms is used:

- $I_L \cdot \hat{d}(s) = 0$

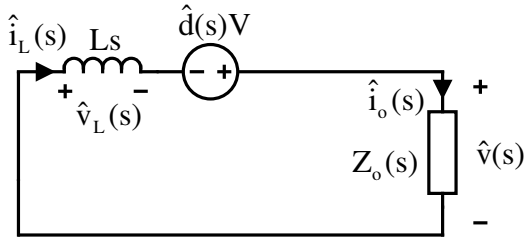


Figure 3.6: *The small signal model when* $I_L \cdot \hat{d}(s) = 0$

$$V \cdot \hat{d}(s) = \hat{i}_L(s) \cdot s \cdot L + \hat{i}_L(s) \cdot Z_o(s) \tag{3.30}$$

$$\hat{v}(s) = \hat{i}_o(s) \cdot Z_o(s) = \frac{\hat{i}_L(s)}{D'} \cdot Z_o(s) \tag{3.31}$$

$$G_{vd1}(s) = \frac{\hat{v}(s)}{\hat{d}(s)} = \frac{V}{D'} \cdot \frac{1}{den(s)} \tag{3.32}$$

$$den(s) = \frac{L \cdot C \cdot s^2}{D^2} + \frac{L \cdot s}{D^2 \cdot R} + 1 \tag{3.33}$$

- $V \cdot \hat{d}(s) = 0$

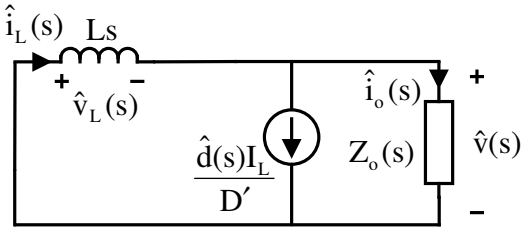


Figure 3.7: *The small signal model when* $V \cdot \hat{d}(s) = 0$

When the $\hat{d}(s) \cdot V$ is zero the Kirchhoff's current law is satisfied if:

$$-\frac{I_L}{D'} \cdot \hat{d}(s) = -\hat{i}_L(s) + \frac{D' \cdot \hat{v}(s)}{Z_o(s)} \tag{3.34}$$

$$-\frac{I_L}{D'} \cdot \hat{d}(s) = \frac{D' \cdot \hat{v}(s)}{L \cdot s} + \frac{D' \cdot \hat{v}(s)}{Z_o(s)} \tag{3.35}$$

Considering the that in steady state the $\frac{I_L}{D'} = \frac{V}{D^2 \cdot R}$ as the capacitor current is equal to zero, the G_{vd} can be written as:

$$G_{vd2}(s) = \frac{\hat{v}(s)}{\hat{d}(s)} = \frac{-\frac{V}{D' \cdot R} \cdot R \cdot L \cdot s}{R \cdot D^2 + L \cdot s + R \cdot L \cdot C \cdot s^2} = \frac{V}{D'} \cdot \frac{-\frac{L \cdot s}{D^2 \cdot R}}{den(s)} \tag{3.36}$$

Adding equation 3.32 to 3.36 the final duty cycle-to-ouput voltage transfer function is obtained:

$$G_{vd}(s)\Big|_{\hat{v}_g(s)=0} = \frac{\hat{v}(s)}{\hat{d}(s)} = \frac{V}{D'} \cdot \frac{1 - \frac{L}{D^2 \cdot R} \cdot s}{den(s)} \tag{3.37}$$

Similarly the effects of the input voltage and duty cycle variations on the inductor current can be analyzed through G_{ig} and G_{id} transfer functions. Consider the ac small signal model shown in Figure 3.4.

To obtain the duty cycle-to-inductor current transfer function, the superposition of the values is used, just as in calculation of the G_{vd} (Figure 3.6 and Figure 3.7).

- $I \cdot \hat{d}(s) = 0$

$$V \cdot \hat{d}(s) = \hat{i}_L \cdot L \cdot s + \hat{i}_L \cdot Z_{out}(s) \tag{3.38}$$

$$G_{id1}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{V}{D^2 \cdot R} \cdot \frac{C \cdot R \cdot s + 1}{den(s)} \tag{3.39}$$

- $V \cdot \hat{d}(s) = 0$

When the V voltage is zero and all the components are transfered to the left side of the model:

$$-\hat{i}_L(s) \cdot L \cdot s = \left(-\frac{I_L \cdot \hat{d}(s)}{D'} + \hat{i}_L \right) \cdot Z_{out}(s) \tag{3.40}$$

$$\hat{i}_L(s) \cdot (L \cdot s + Z_{out}(s)) = \frac{I_L \cdot Z_{out}(s) \cdot \hat{d}(s)}{D'} \tag{3.41}$$

$$G_{id2}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{\frac{I_L}{D'} \cdot \frac{D^2 \cdot R}{R \cdot C \cdot s + 1}}{\frac{L \cdot R \cdot C \cdot s^2 + L \cdot s + D^2 \cdot R}{R \cdot C \cdot s + 1}} = \frac{V}{D^2 \cdot R} \cdot \frac{1}{den(s)} \tag{3.42}$$

Adding equation 3.39 to 3.42:

$$G_{id}(s)\Big|_{\hat{v}_g(s)=0} = \frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{2 \cdot V}{D^2 \cdot R} \cdot \frac{\frac{R \cdot C}{2} \cdot s + 1}{den(s)} \tag{3.43}$$

3.2.2 Modeling of an interleaved boost converter

In order to design a proper control, an accurate small signal model of the interleaved boost converter is needed. The converter is operated in continuous conduction mode with the same duty cycle for both legs. The only difference between the two legs is that the duty cycle is shifted in time with half switching period. Similarly like in Section 3.2.1.1, the converter model can be defined in two switching states for each legs. Averaging the

the inductor voltage and capacitor current values over one switching period, the flowing equations are obtained.

$$L_1 \cdot \frac{d\left\langle i_{L1}(t)\right\rangle_{T_s}}{dt} = \left\langle v_g(t)\right\rangle_{T_s} - d'(t) \cdot \left\langle v(t)\right\rangle_{T_s} \tag{3.44}$$

$$L_2 \cdot \frac{d\left\langle i_{L2}(t)\right\rangle_{T_s}}{dt} = \left\langle v_g(t)\right\rangle_{T_s} - d'(t) \cdot \left\langle v(t)\right\rangle_{T_s} \tag{3.45}$$

$$C \cdot \frac{d\left\langle v(t)\right\rangle_{T_s}}{dt} = d'(t) \cdot \left(\left\langle i_{L1}(t)\right\rangle_{T_s} + \left\langle i_{L2}(t)\right\rangle_{T_s}\right) - \frac{\left\langle v(t)\right\rangle_{T_s}}{R} \tag{3.46}$$

$$\left\langle i_L(t)\right\rangle_{T_s} = d'(t) \cdot \left(\left\langle i_{L1}(t)\right\rangle_{T_s} + \left\langle i_{L2}(t)\right\rangle_{T_s}\right) \tag{3.47}$$

As the duty cycle is the same the term $d'(t)$ is also identical for both legs. Differences between the model of the two legs can appear only due to the inductor values (L_1 and L_2).

Linearizing the above differential equations with the same technique used in Section 3.2.1.2 one will get:

$$L_1 \cdot \frac{d\hat{i}_{L1}(t)}{dt} = \hat{v}_g(t) + \hat{d}(t) \cdot V - D' \cdot \hat{v}(t) \tag{3.48}$$

$$L_2 \cdot \frac{d\hat{i}_{L2}(t)}{dt} = \hat{v}_g(t) + \hat{d}(t) \cdot V - D' \cdot \hat{v}(t) \tag{3.49}$$

$$C \cdot \frac{d\hat{v}(t)}{dt} = D' \cdot (\hat{i}_{L1}(t) + \hat{i}_{L2}(t)) - \hat{d}(t) \cdot (I_{L1} + I_{L1}) - \frac{\hat{v}(t)}{R} \tag{3.50}$$

$$\hat{i}_L(t) = D' \cdot (\hat{i}_{L1}(t) + \hat{i}_{L2}(t)) - \hat{d}(t) \cdot (I_{L1} + I_{L1}) \tag{3.51}$$

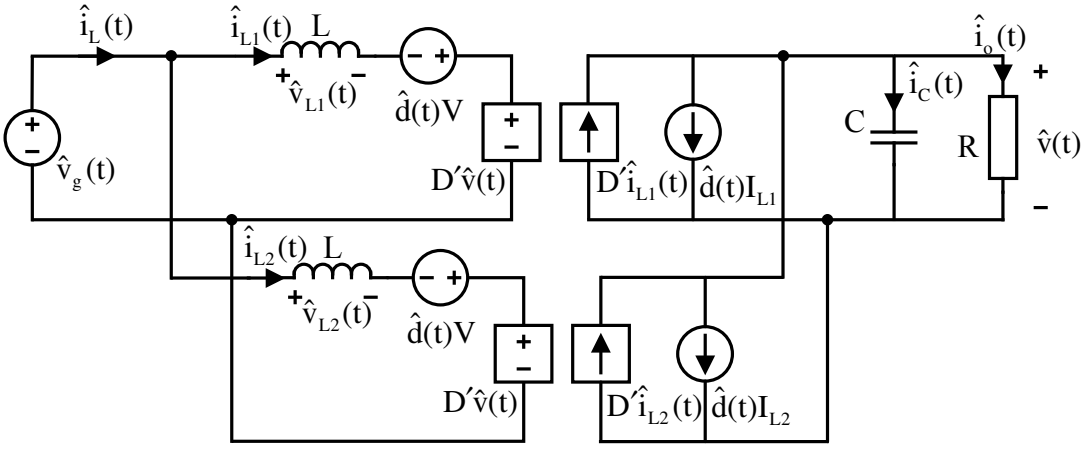


Figure 3.8: *Small signal model of an interleaved boost converter*

Many terms are duplicated in the two legs (Figure 3.8). It is possible to simplify the model by extracting the common components on a main leg. The result is almost like the simple boost model. The two differences are the paralleled inductors and the two current sources merged into one (Figure 3.9).

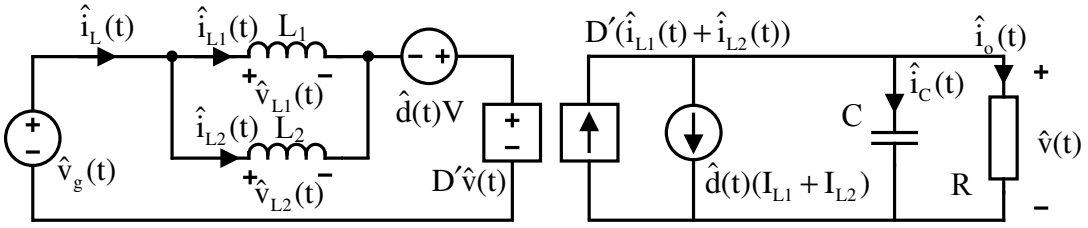


Figure 3.9: *Simplified small signal model of an interleaved boost converter*

To control the inductor current, the sum of the two inductor currents is measured and used as feedback. Thus a simplification can be also introduced to eliminate the unnecessary current terms. As $\hat{i}_L(t) = \hat{i}_{L1}(t) + \hat{i}_{L2}(t)$ and $I_L = I_{L1} + I_{L2}$, the final model of the interleaved boost converter in frequency domain is presented in Figure 3.10. This control solution was chosen because of its implementation is easier with the 16bit fixed point digital signal processor. The problem of current sharing can be solved by limiting the tolerance of the components (inductors, gate drivers, MOSFETs).

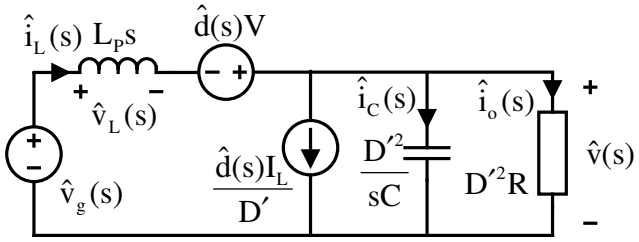


Figure 3.10: *Small signal model of an interleaved boost converter in frequency domain*

The transfer functions of an interleaved boost converter are identical to the simple boost converter ones. The single exception is represented by the inductor term in using the paralleled value L_p.

$$G_{vg}(s)\Big|_{\hat{d}(s)=0} = \frac{\hat{v}(s)}{\hat{v}_g(s)} = \frac{1}{D'} \cdot \frac{1}{deni(s)} \tag{3.52}$$

$$G_{vd}(s)\Big|_{\hat{v}_g(s)=0} = \frac{\hat{v}(s)}{\hat{d}(s)} = \frac{V}{D'} \cdot \frac{1 - \frac{L_p}{D'^2 \cdot R} \cdot s}{deni(s)} \tag{3.53}$$

$$G_{ig}(s)\Big|_{\hat{d}(s)=0} = \frac{\hat{i}_L(s)}{\hat{v}_g(s)} = \frac{1}{D'^2 \cdot R} \cdot \frac{C \cdot R \cdot s + 1}{deni(s)} \tag{3.54}$$

$$G_{id}(s)\Big|_{\hat{v}_g(s)=0} = \frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{2 \cdot V}{D'^2 \cdot R} \cdot \frac{\frac{R \cdot C}{2} \cdot s + 1}{deni(s)} \tag{3.55}$$

$$deni(s) = \frac{L_p \cdot C \cdot s^2}{D^2} + \frac{L_p \cdot s}{D^2 \cdot R} + 1 \tag{3.56}$$

3.2.3 Modeling of phase-shifted full-bridge converter with current doubler

To model a phase-shifted full-bridge converter first it is necessary to understand how does it work. The four MOSFETs of the primary side are operated with fixed duty cycle gate signals (around 50% of the switching period). The dead time between the turn-off time of he high and turn-on time of the low transistor (and inverse) has to be determined in such a way that it allows enough time to charge and discharge the internal capacitors of the switching devices.

The second leg is switched phase shifted in time compared to the first leg's pulses. The overlap between the two phases determines the duty cycle of the input voltage on the transformer. It the phase shift reaches the 50% of the switching period the converter behaves like a simple full bridge converter without zero voltage switching. If the phase shift is 0 than no power is transfer to the secondary side. The output voltage can be calculated as:

$$V = V_g \cdot \frac{N_s}{N_p} \cdot D_{eff} \tag{3.57}$$

where V is the output voltage of the converter, N_s and N_p are the number of turns in the secondary and primary windings of the transformer, V_g is the input voltage and D_{eff} is the effective duty cycle.

Detailed operation has been described in many publications [73]-[79]. The basic idea is to achieve zero voltage switching in the full-bridge MOSFETs. The mode how to reached this is to discharge the MOSFET's internal capacitors before the transistor turns on, thus the anti parallel diodes start conducting (Fugure 3.11). The role of the small C_b blocking capacitor is to reduce rapidly the primary current when V_p is 0 [79].

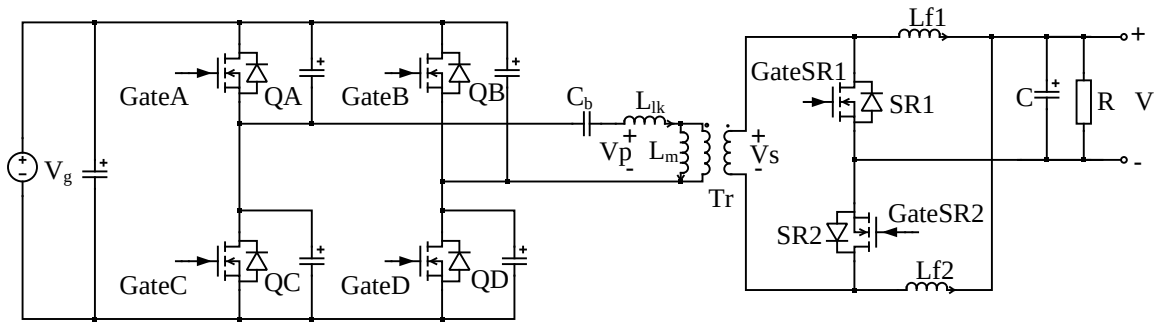


Figure 3.11: *Schematic of the phase-shifted full-bridge converter with current doubler*

To make the small signal model of the converter only few steps in operation are highlighted. Firstly the duty cycle has to be examined in order to calculate the duty

cycle-to-filter inductor current and duty cycle-to-output voltage transfer functions. The fact that it is determined by the phase shift between the two legs makes the duty cycle sensitive to hardware parameter changes. As shown in 3.58 and Figure 3.12 the effective duty cycle (D_{eff}) is smaller than the the one obtained from the phase-shift (D). ΔD appears due to the finite slopes of the primary current. To obtain the required output voltage calculated in 3.57, D has to be compensated to eliminate the effect caused by ΔD.

$$D_{eff} = D - \Delta D \tag{3.58}$$

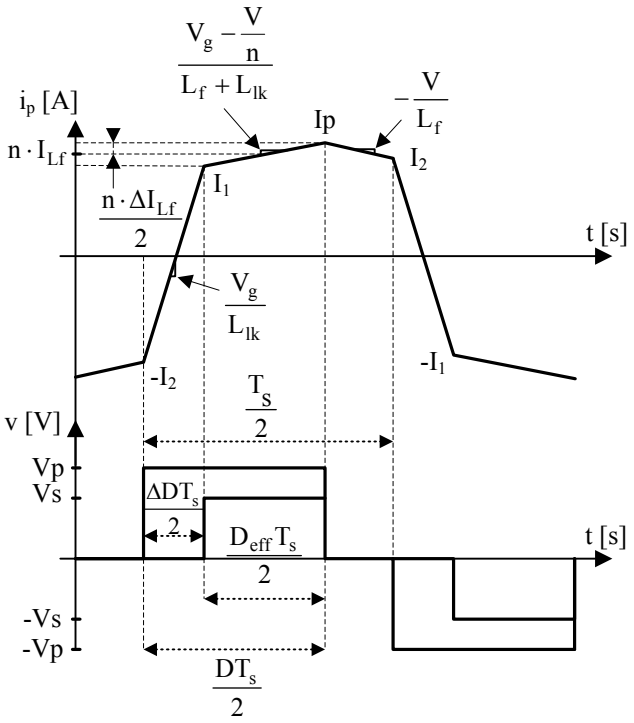


Figure 3.12: *Primary current, primary and secondary voltage waveforms [74]*

To deliver the required output power the right value of the necessary phase-shift has to be calculated. Thus it is necessary to estimate the deviation ΔD by analyzing Figure 3.12.

$$\begin{aligned} I_1 &= n \cdot \left(I_{Lf} - \frac{\Delta I_{Lf}}{2} \right) \\ I_2 &= n \cdot \left(\underbrace{I_{Lf} + \frac{\Delta I_{Lf}}{2}}_{I_p} - (1 - D) \cdot \frac{V}{L_f} \cdot \frac{T_s}{2} \right) \end{aligned} \tag{3.59}$$

where $n = \frac{N_s}{N_p}$, being the ration between the number of turns of the transformer. As the converter has a current doubler on the output, $I_{Lf} = I_{load}/2$ is the average current

in the transformer during half time of the switching period T_s. ΔI_{Lf} is the filter inductor (L_f) peak-to-peak current ripple. From Figure 3.12 one can determine ΔD:

$$\Delta D \cdot \frac{T_s}{2} = \frac{I_1 + I_2}{\frac{V_g}{L_{lk}}} \text{ thus}$$
$$\Delta D = \frac{I_1 + I_2}{\frac{V_g}{L_{lk}} \cdot \frac{T_s}{2}} \tag{3.60}$$

Combining equation 3.59 and 3.60 the ΔD becomes:

$$\Delta D = \frac{n}{\frac{V_g}{L_{lk}} \cdot \frac{T_s}{2}} \cdot \left(2 \cdot I_{Lf} - (1 - D) \cdot \frac{V}{L_f} \cdot \frac{T_s}{2}\right) \tag{3.61}$$

Substituting the obtained formula from 3.61 for ΔD in equation 3.58 and using 3.57, the actual phase-shift can be calculated:

$$D = \underbrace{\frac{V}{V_g} \cdot \frac{1}{n}}_{D_{eff}} + \underbrace{\frac{n}{\frac{V_g}{L_{lk}} \cdot \frac{T_s}{2}} \cdot \left(2 \cdot I_{Lf} - (1 - D) \cdot \frac{V}{L_f} \cdot \frac{T_s}{2}\right)}_{\Delta D} \tag{3.62}$$

The filter inductor current can be written in form of the ration of the output voltage and load resistance:

$$2 \cdot I_{Lf} = I_{load} = \frac{V}{R} \tag{3.63}$$

With this modification 3.62 becomes:

$$D \cdot \left(1 - \frac{\frac{1}{n} \cdot \frac{V}{V_g}}{\frac{L_f}{L_{lk}} \cdot \frac{T_s}{2}} \cdot \frac{T_s}{2}\right) = \frac{V}{V_g} \cdot \frac{1}{n} + \frac{n \cdot \frac{V}{V_g}}{\frac{R}{L_{lk}} \cdot \frac{T_s}{2}} - \frac{n \cdot \frac{V}{V_g}}{\frac{L_f}{L_{lk}} \cdot \frac{T_s}{2}} \cdot \frac{T_s}{2} \tag{3.64}$$

$$D = \frac{D_{eff} + \frac{n^2 \cdot D_{eff} \cdot 2 \cdot f_s}{\frac{R}{L_{lk}}} - \frac{n^2 \cdot D_{eff}}{\frac{L_f}{L_{lk}}}}{\left(1 - \frac{n^2 \cdot D_{eff}}{\frac{L_f}{L_{lk}}}\right)} \tag{3.65}$$

The simplified equation of D:

$$D = \frac{1 + \frac{n^2 \cdot 2 \cdot f_s \cdot L_{lk}}{R} - \frac{n^2 \cdot L_{lk}}{L_f}}{\frac{1}{D_{eff}} - \frac{n^2 \cdot L_{lk}}{L_f}} \tag{3.66}$$

To calculate the optimal duty cycle, thus the right shifting, one should consider its dependency on the leakage inductance of the transformer (L_{lk}), the output filter inductance (L_f), the switching frequency (f_s), load resistance (R) and the transformer turns ratio (n) [74].

The duty cycle variation is controlled by changing the shift value between the two legs.

Two other factors might also modify the effective value of the duty cycle. If there is s a small rise in the filter inductor current ($\hat{i}_{Lf}$), the duty cycle might decrease with time Δt (Figure 3.13 a.)). If there is a small increase in the input voltage ($\hat{v}_g$) on the primary side (Vp), the slope of the transformer will become steeper thus the duty cycle will increase also with a time Δt (Figure 3.13 b.)) [73].

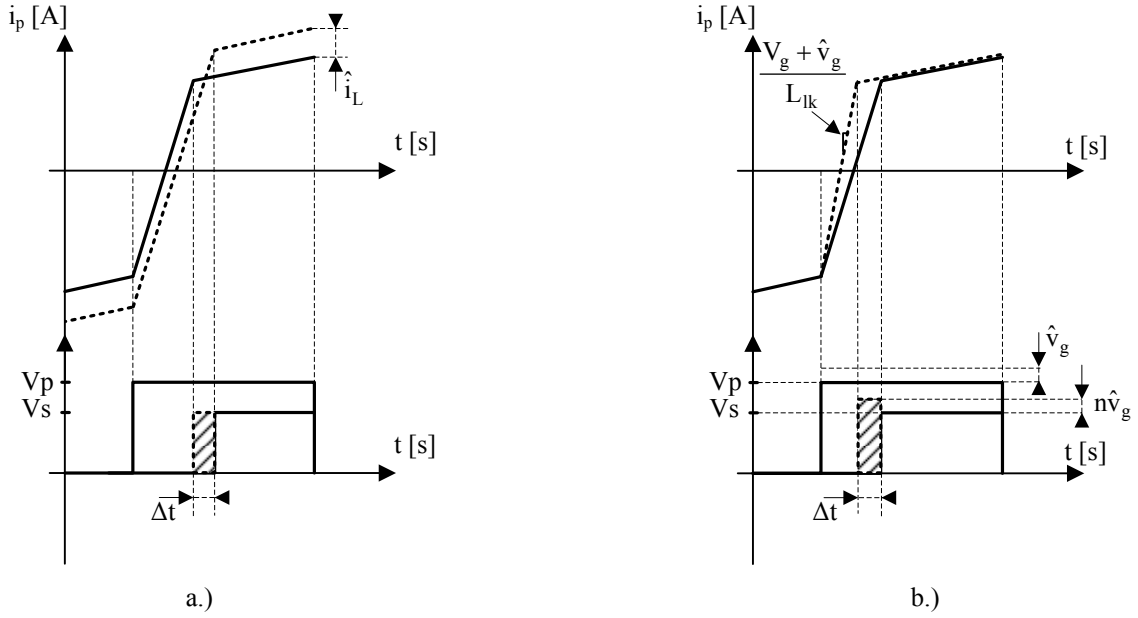


Figure 3.13: *Duty cycle variation due to: a.) changes in filter inductor current; b.) changes in input voltage [74]*

The two factors representing the impact of $\hat{i}_{Lf}$ and $\hat{v}_g$ ($\hat{d}_i$ and $\hat{d}_v$) will be added to the $\hat{d}_{eff}$ when calculating the linearized model.

From Figure 3.13 a.) one can write [74]:

$$\Delta D \cdot \frac{T_s}{2} + \Delta t = \frac{(I_1 + I_2) + 2 \cdot n \cdot \hat{i}_{Lf}}{\frac{V_g}{L_{lk}}}$$

$$\Delta t = + \frac{2 \cdot n \cdot \hat{i}_{Lf}}{\frac{V_g}{L_{lk}}} \tag{3.67}$$

The value of $\hat{d}_i$ is:

$$\hat{d}_i = \frac{\Delta t}{\frac{T_s}{2}} = \frac{4 \cdot n \cdot L_{lk}}{V_g \cdot T_s} \cdot \hat{i}_{Lf} \tag{3.68}$$

and it is dependent on the turns ratio (n) and leakage inductance (L_{lk}) of the transformer, the input voltage (V_g), switching frequency ($f_s = \frac{1}{T_s}$) and the filter inductor current perturbation ($\hat{i}_{Lf}$).

Similarly from Figure 3.13 b.) the duty cycle deviation (ΔD) can be written:

$$\Delta D \cdot \frac{T_s}{2} - \Delta t = \frac{(I_1 + I_2)}{\frac{V_g + \hat{v}_g}{L_{lk}}} \tag{3.69}$$

Combining equation 3.59 and 3.69 it results:

$$\Delta t = n \cdot \left(2 \cdot I_{Lf} - (1 - D) \cdot \frac{V}{L_f} \cdot \frac{T_s}{2}\right) \cdot \left(\frac{L_{lk}}{V_g} - \frac{L_{Lk}}{V_g + \hat{v}_g}\right) \tag{3.70}$$

Simplifying the above equation and assuming that $2 \cdot I_{Lf} >> (1 - D) \cdot \frac{V}{L_f} \cdot \frac{T_s}{2}$ as the term $1 - D$ is minimized for to get maximum power transfer [73]:

$$\Delta t = n \cdot 2 \cdot I_{Lf} \cdot \frac{L_{lk} \cdot \hat{v}_g}{V_g \cdot (V_g + \hat{v}_g)} \tag{3.71}$$

Assuming that $V_g + \hat{v}_g \approx V_g$ under small signal conditions, the $\hat{d}_v$ can be expressed as:

$$\hat{d}_v = \frac{\Delta t}{\frac{T_s}{2}} = n \cdot 4 \cdot I_{Lf} \cdot \frac{L_{lk}}{{V_g}^2 \cdot T_s} \cdot \hat{v}_g \tag{3.72}$$

The phase-shifted full-bridge converter is basically an isolated step-down converter. It can be modeled as a simple buck converter [73]. As it has current doubler and synchronous rectifier therefore it can be interpreted as an interleaved synchronous buck converter (Figure 3.14). The voltage $n \cdot V_g$ is the secondary voltage V_s on the transformer, representing the input voltage to the interleaved synchronous buck converter. The $Q1$ and $Q2$ MOSFETs are switched with T_s and the duty cycle is the required D_{eff} calculated in 3.58. The two gate signals are shifted with half of the switching period. The $SR1$ and $SR2$ are the synchronous rectifiers from Figure 3.11 and are switched with the same pulse as $GateC$ and $GateA$.

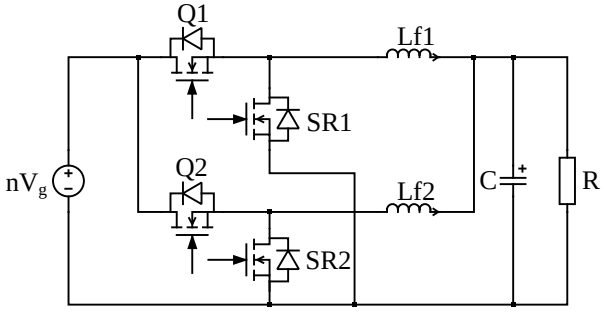


Figure 3.14: *Interleaved synchronous buck converter*

To compare the two topologies two models have been built in Matlab/Simulik and PLECS environment. The results waveforms are presented in Figure 3.15.

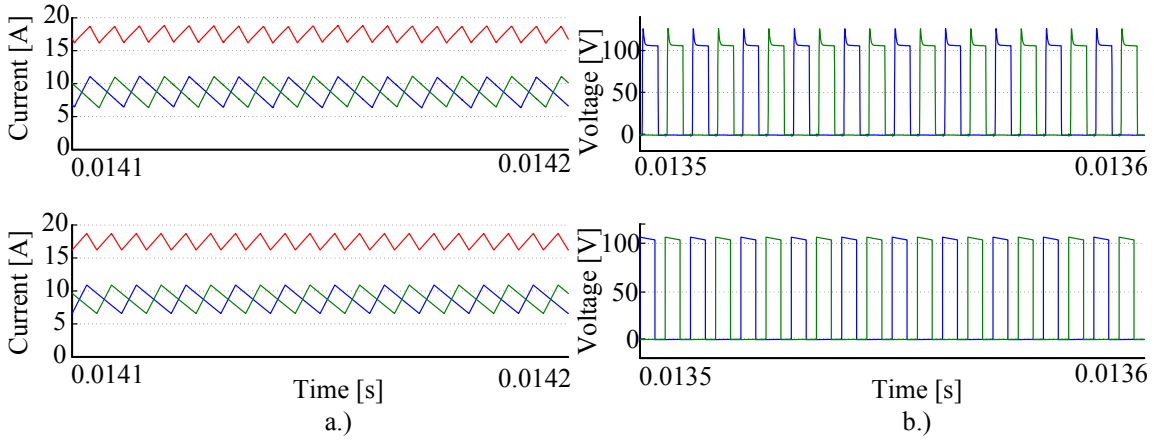


Figure 3.15: *Current and drain-source voltage waveforms*

Figure 3.15 a.) shows two sets of current waveforms. The upper set presents the phase-shifted full-bridge converter output filter inductor ($Lf1$ and $Lf2$) currents (blue and green) and being a current doubler the sum of them (red). The bottom set shows the inductor currents of the interleaved synchronous buck converter. Figure 3.15 b.) presents the drain source voltages from the synchronous rectifier ($SR1$ and $SR2$) of the full bridge converter (upper set) and the buck converter (lower set).

Based on the above comparison the small signal model of phase-shifted full-bridge converter with current doubler will be developed as it would be a synchronous buck converter. Averaging the inductor voltage and capacitive current values over the switching period, the differential equations, which describe the converter operation are:

$$Lf1 \cdot \frac{d\left\langle i_{Lf1}(t)\right\rangle_{T_s}}{dt} = d_{eff}(t) \cdot n \cdot \left\langle v_g(t)\right\rangle_{T_s} - \left\langle v(t)\right\rangle_{T_s} \tag{3.73}$$

$$Lf2 \cdot \frac{d\left\langle i_{Lf2}(t)\right\rangle_{T_s}}{dt} = d_{eff}(t) \cdot n \cdot \left\langle v_g(t)\right\rangle_{T_s} - \left\langle v(t)\right\rangle_{T_s} \tag{3.74}$$

$$C \cdot \frac{d\left\langle v(t)\right\rangle_{T_s}}{dt} = \left\langle i_{Lf1}(t)\right\rangle_{T_s} + \left\langle i_{Lf2}(t)\right\rangle_{T_s} - \frac{\left\langle v(t)\right\rangle_{T_s}}{R} \tag{3.75}$$

$$\left\langle i_g(t)\right\rangle_{T_s} = d_{eff}(t) \cdot \left(\left\langle i_{Lf1}(t)\right\rangle_{T_s} + \left\langle i_{Lf2}(t)\right\rangle_{T_s}\right) \tag{3.76}$$

For linearizing the above differential equations around a specific operational point, the same technique is used that was presented in Section 3.2.1.2. A small perturbation is introduced and added to the steady state variables of the synchronous buck converter.

$$\left\langle i_{Lf1}(t)\right\rangle_{T_s} = I_{Lf1} + \hat{i}_{Lf1}(t) \tag{3.77}$$

$$\left\langle i_{Lf2}(t)\right\rangle_{T_s} = I_{Lf2} + \hat{i}_{Lf2}(t) \tag{3.78}$$

$$\left\langle v(t)\right\rangle_{T_s} = V + \hat{v}(t) \tag{3.79}$$

$$n \cdot \langle v_g(t) \rangle_{T_s} = n \cdot (V_g + \hat{v}_g(t)) \tag{3.80}$$

$$\langle d_{eff}(t) \rangle_{T_s} = D_{eff} + \hat{d}_{eff}(t) \tag{3.81}$$

Combining equations 3.73-3.76 with 3.77-3.81 and neglecting the DC and 2^{nd} order components, the resulting linear equations :

$$Lf1 \cdot \frac{d\hat{i}_{Lf1}(t)}{dt} = \hat{d}_{eff}(t) \cdot n \cdot V_g - D_{eff} \cdot n \cdot \hat{v}_g(t) - \hat{v}(t) \tag{3.82}$$

$$Lf2 \cdot \frac{d\hat{i}_{Lf2}(t)}{dt} = \hat{d}_{eff}(t) \cdot n \cdot V_g - D_{eff} \cdot n \cdot \hat{v}_g(t) - \hat{v}(t) \tag{3.83}$$

$$C \cdot \frac{d\hat{v}(t)}{dt} = \hat{i}_{Lf1}(t) + \hat{i}_{Lf2}(t) - \frac{\hat{v}(t)}{R} \tag{3.84}$$

$$\hat{i}_g(t) = \hat{d}_{eff}(t) \cdot (I_{Lf1} + I_{Lf2}) + D_{eff}(t) \cdot \left(\hat{i}_{Lf1}(t) + \hat{i}_{Lf2}(t) \right) \tag{3.85}$$

The small signal model of the synchronous buck converter, based on the linear equations 3.82-3.85, is shown in Figure 3.16.

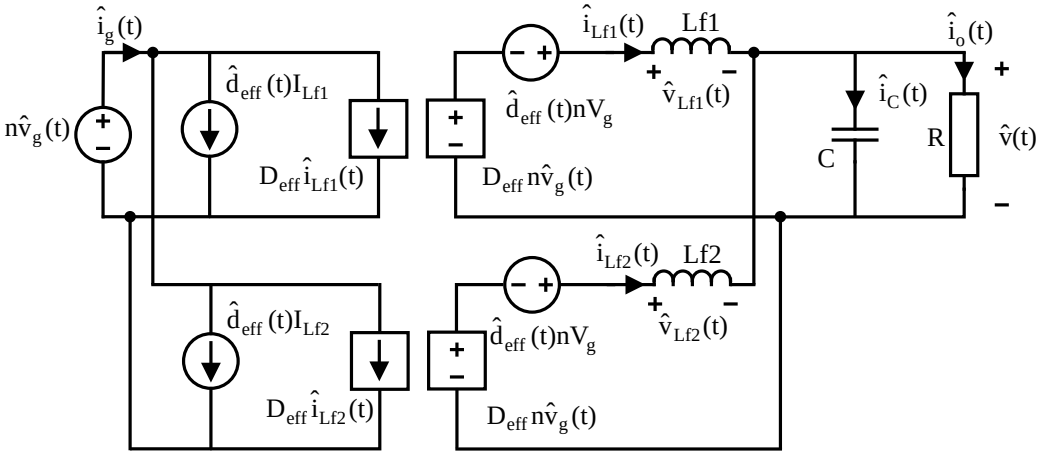


Figure 3.16: *Small signal model of a synchronous buck converter*

There are two current path ($\hat{i}_{Lf1}$ and $\hat{i}_{Lf2}$) but both of them have identical elements. Contracting these independent voltage and current sources the result is presented in Figure 3.17. In steady state conditions the the sum of the two filter inductor currents is equal to the output current: $I_{Lf1} + I_{Lf2} = I_o$. The result model differs from the simple buck converter in the output paralleled filter inductors.

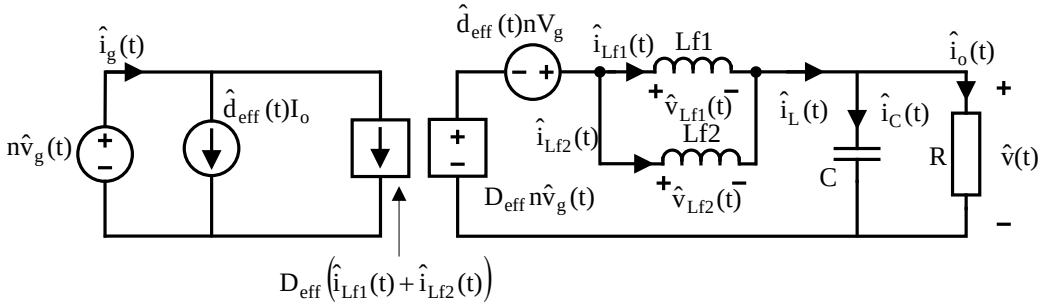


Figure 3.17: *Contracted small signal model of a synchronous buck converter*

By transferring all the components to one side of the DC transformer the calculations can be simplified. The chosen side depends on where the variables which needs to be controlled are. In this particular case the right side is chosen due to the fact that the sum of the inductor currents and the output voltage has to be controlled (Figure 3.18)

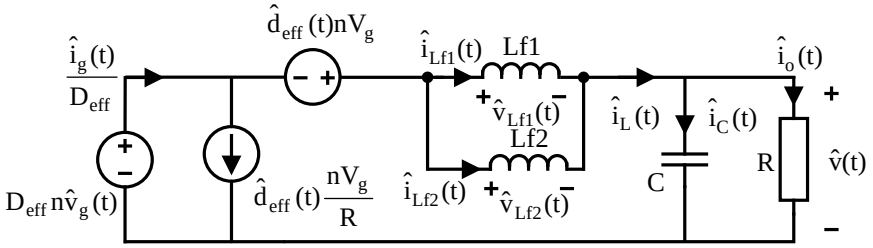


Figure 3.18: *Simplified small signal model of a synchronous buck converter*

What makes the phase-shifted full-bridge converter different from the synchronous interleaved buck converter is the perturbation of the duty cycle. As presented in Figure 3.13, beside the actual shift perturbation the small change in the output inductor current and the input voltage will affect the effective duty cycle variation.

$$\hat{d}_{eff}(t) = \hat{d}(t) - \hat{d}_i(t) + \hat{d}_v(t) \tag{3.86}$$

where $\hat{d}(t)$ is the programmed shift variation and $\hat{d}_i(t)$ and $\hat{d}_v(t)$ are the variations due to parameter changes, discussed earlier (Equations 3.68 and 3.72) The term $\hat{d}_i(t)$ is with '$-$' because the the increase of the inductor current will reduce and a decrease of it will increase the effective duty cycle. Figure 3.19 includes also the additional factors, represented by a dependent voltage and a current source. As the two additional components act on the secondary side, the transformer turns ratio must be introduced in the:

$$\hat{d}_i = \frac{4 \cdot n \cdot L_{lk}}{n \cdot V_g \cdot T_s} \cdot \hat{i}_{Lf} \tag{3.87}$$

$$\hat{d}_v = n \cdot 4 \cdot I_{Lf} \cdot \frac{L_{lk}}{n^2 \cdot {V_g}^2 \cdot T_s} \cdot \hat{v}_g \tag{3.88}$$

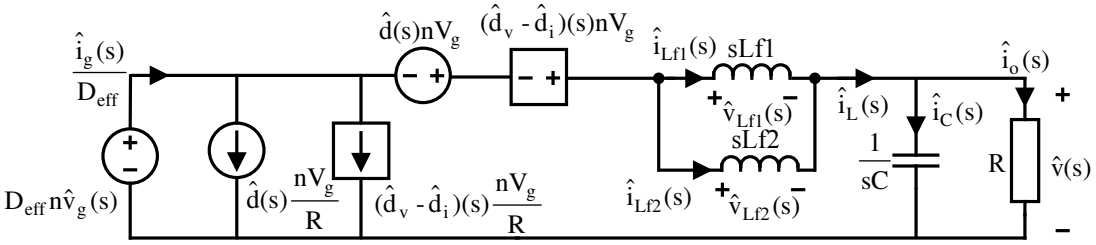


Figure 3.19: *Small signal model of a synchronous buck converter in 's' domain*

Having built the small signal model of the phase-shifted full-bridge converter, the duty cycle-to-inductor current and duty cycle-to-output voltage can be determined the same way as presented in Section 3.2.1.3.

When calculating the control to current or voltage transfer functions the other inputs are considered zero ($\hat{v}_g = 0$).

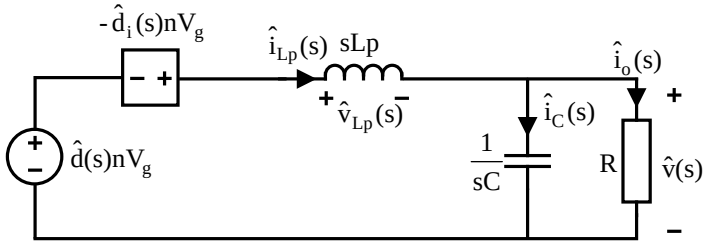


Figure 3.20: *Simplified small signal model of a synchronous buck converter in 's' domain*

From the above model the Kirchhoff's voltage law:

$$\hat{d}(s) \cdot n \cdot V_g = \hat{d}_i \cdot n \cdot V_g + \hat{i}_{Lp} \cdot s \cdot Lp + \hat{i}_{Lp} \cdot Zo \tag{3.89}$$

where

$$Zo = \frac{R}{C \cdot R \cdot s + 1} \tag{3.90}$$

and $\hat{d}_i$ is determined in equation 3.87. Thus the duty cycle-to-inductor current transfer function is:

$$G_{id}(s)\Big|_{\hat{v}_g(s)=0} = \frac{\hat{i}_{Lp}(s)}{\hat{d}(s)} = \frac{n \cdot V_g}{R} \cdot \frac{C \cdot R \cdot s + 1}{L \cdot C \cdot s^2 + (Z_b \cdot C + \frac{Lp}{R}) \cdot s + \frac{Z_b}{R} + 1} \tag{3.91}$$

where $Z_b = 2 \cdot n \cdot L_{lk} \cdot f_s$, and $2 \cdot \hat{i}_{Lf} = \hat{i}_{Lp}$.

Similarly the the Kirchhoff's voltage law is used to determine the duty cycle-to-output

voltage transfer function:

$$\hat{d}(s)\cdot n\cdot V_g=\left(\frac{2\cdot n\cdot L_{lk}\cdot f_s}{n\cdot V_g}\cdot n\cdot V_g+Lp\cdot s\right)\cdot\left(\underbrace{C\cdot\hat{v}(s)\cdot s+\frac{\hat{v}(s)}{R}}_{\hat{i}_{Lp}(s)}\right)+\hat{v}(s) \tag{3.92}$$

Simplifying the above equation, the duty cycle-to-output voltage transfer function is:

$$G_{vd}(s)\Big|_{\hat{v}_g(s)=0}=\frac{\hat{v}(s)}{\hat{d}(s)}=n\cdot V_g\cdot\frac{1}{L\cdot C\cdot s^2+(Z_b\cdot C+\frac{Lp}{R})\cdot s+\frac{Z_b}{R}+1} \tag{3.93}$$

By calculating analytically the linear duty cycle-to-inductor current and duty cycle-to-output voltage transfer functions for different converters the traditional linear control methods can be applied. To design the controller in the discrete domain, different model discretizing techniques exists as follows.

3.2.4 Model discretization

One solution to design digital controllers is to treat the model as discrete system. As presented earlier the system transfer functions are derived in continuous domain. Different techniques exist to perform discretization.

A solution is to emulate the hold circuit from the analog-to-digital converter. The $Zero-order-hold$ (ZOH) and $First-order-hold$ (FOH) methods are using the impulse signal as sampler and a holding operation to determine the discrete value during one sampling time unit. The drawback in analytical calculations is that these two methods introduce additional Z transform operations making harder the calculations (3.94).

$$\begin{aligned} G(z)&=(1-z^{-1})\cdot Z\left\{\frac{G(s)}{s}\right\}\text{ - for ZOH}\\ G(z)&=\frac{1-z^{-1}}{T_s}\cdot Z\left\{\frac{G(s)}{s^2}\right\}\text{ - for FOH}\end{aligned} \tag{3.94}$$

Numerical integration methods make possible transformation only by replacing s in the transfer functions with its discrete equivalent. Three possible solutions are discussed in the literature. The $Euler-Forward$ method approximates the sampled value being constant until the next sampling time. The $Euler-Backward$ method considers the sampled value constant between the previous and current sampling. The $Bilinear\ transformation$ or $Trapezoidal$ method takes the average value between the previous and current sample.

The $Euler-Forward$ method is mapping from s plain to z domain only by shifting the origin. This means that the whole left half plain from frequency domain will be shifted right with the origin in (1,0) in discrete domain. This might result in mapping some stable s poles to unstable area in z domain [80]. The $Euler-Backward$ transformation narrows the negative s plain into a circle with radius 0.5 and origin at (0.5,0). The major advantage of the $Trapezoidal$ $(Tustin)$ method is that it maps the whole left half plain in s domain

into the whole circle with unity radius and center at (0,0), thus mapping the stable area from frequency domain into the stable area of the z plain.

Comparison of $Tustin$, ZOH and FOH is shown in Figure 3.21

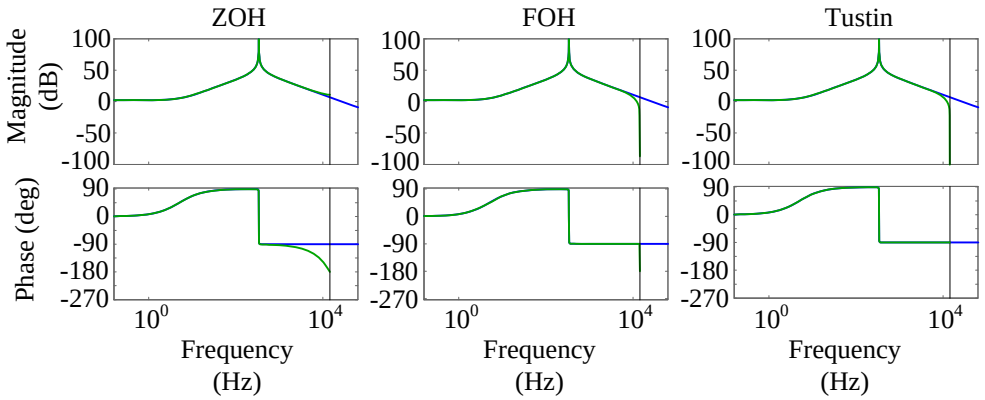


Figure 3.21: *Bode plot of the continuous and discrete system with different discretization methods*

As shown, the bode plot with $Tustin$ ($Bilinear\ transformation$) method follows the best the continuous phase even at high frequencies, though it has a small gain deviation (just as in case of FOH) around the Nyquist frequency.

The present work is will use the $Bilinear\ transformation$.

$$\frac{1}{s} = \frac{T_s}{2} \cdot \frac{z+1}{z-1} \tag{3.95}$$

where T_s is the sampling time. Thus s becomes:

$$s = \frac{2}{T_s} \cdot \frac{z-1}{z+1} \tag{3.96}$$

3.3 Chosen control solutions

The basic current mode control structure of switched-mode power supplies is presented in Figure 3.22.

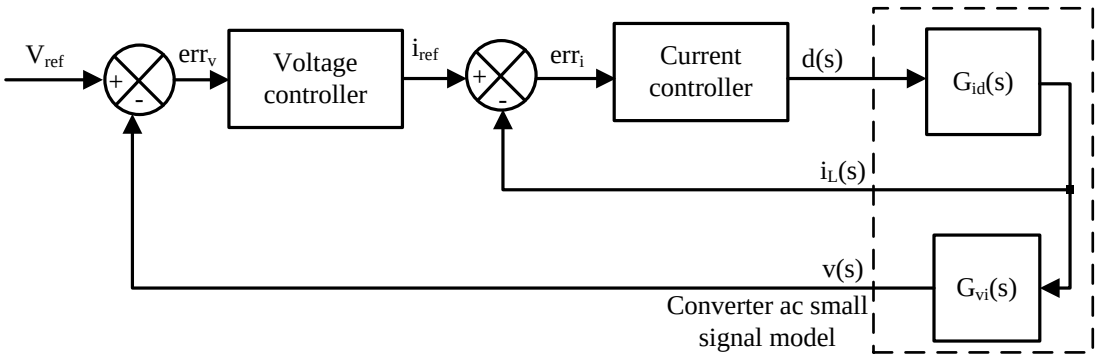


Figure 3.22: *Basic control structure of a power converter*

It can be derived analytically by using the classical transfer function operations, that the above structure is identical to the one presented on Figure 3.23:

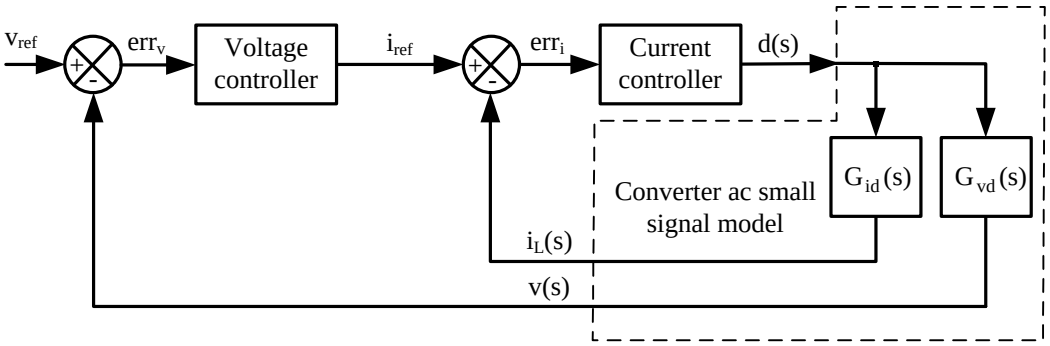


Figure 3.23: *Control structure of a power converter, using duty cycle as control variable*

Current mode control structure was chosen to be implemented in digital controller because it is easy to make stable control loops with high bandwidth. Also current protection can be easily implemented in software. The variation in input voltage does not have effect on the output voltage (lower bandwidth voltage loop) because it is compensated by the fast current loop with fast duty cycle adjustment.

The major focus in the further discussion is on control strategies which can be implemented in digital signal processors and require simple additional circuitry and fixed switching frequency.

3.3.1 Linear PI controller

The *Proportional* and *Integrator* (PI) controller is the most commonly used control method in power electronics. This is because it behaves as a low pass filter and attenuates high frequency noises. It also brings improvement in steady-state error. This advantage is penalized in transient rise time. To improve transient behavior a *Derivative* component could be added to the PI system, resulting in a PID controller. The disadvantage of the derivative is that it behaves like a high pass filter. The high frequency switching noises in power converter applications would make the controller unstable, thus the derivative component is neglected and only PI part is used. In continuous domain the transfer function of the PI controller looks like:

$$G_c(s) = \frac{u(s)}{e(s)} = Kp + \frac{1}{Ti \cdot s} \tag{3.97}$$

where $u(s)$ is the control signal, the output of the controller, while e(s) is the error, the difference between the measured and the reference values. Kp is the proportional gain and Ti is the time constant of the integrator.

Using equation 3.95 the discrete PI controller can be written as:

$$G_c(z) = \frac{u(z)}{e(z)} = Kp + Ki \cdot \frac{z+1}{z-1} \tag{3.98}$$
$$Ki = \frac{T_s}{2 \cdot T_i}$$

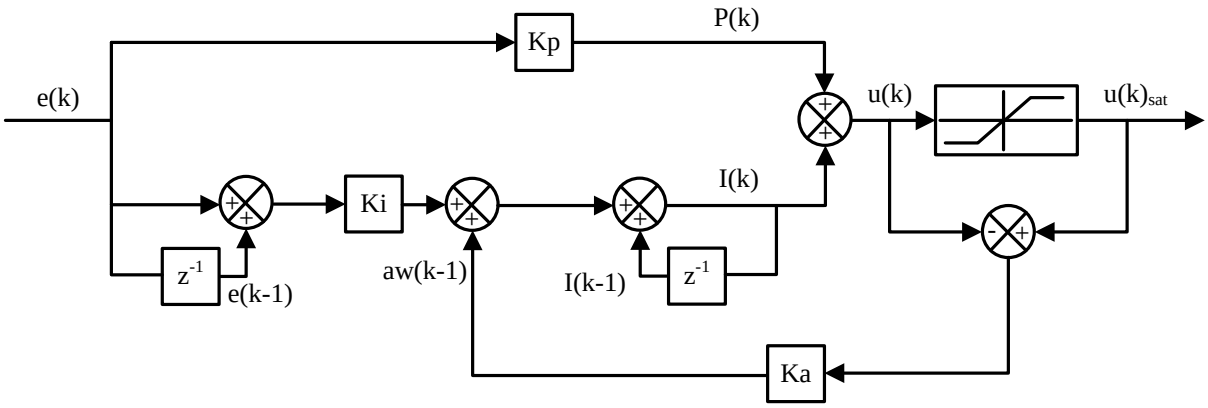


Figure 3.24: *PI control structure*

Figure 3.24 presents the control structure described by equation 3.98. Considering the Z transform properties the implemented control algorithm can be written as:

$$I(k) = I(k-1) + Ki \cdot (e(k) + e(k-1)) + aw(k-1) \tag{3.99}$$
$$P(k) = Kp \cdot e(k)$$
$$u(k) = P(k) + I(k)$$
$$aw(k-1) = Ka \cdot (u(k)_{sat} - u(k)) \tag{3.100}$$

To overcome the windup phenomenon which might occur in the integrator after saturating the controller output, different anti-windup solutions were proposed in literature [97]-[100]. One solution could be to simply saturate the integrator output. To obtain a dynamic solution a tracking anti-windup calculator is used which feeds back to the integrator the difference between the saturated and the calculated output. Between the saturation limits the $aw(k-1)$ is equal to zero. When the high saturation level is reached the difference becomes negative and this value with a gain Ka is subtracted from the integrated value. If the output reaches the negative saturation level, meaning that the integrator went negative, the positive difference is added to it. All this is done to keep the integrator value close to the level where the output had saturated thus avoiding the windup phenomenon. The gain Ka is generally set to be equal to Ki to damp the integrator speed.

3.3.2 Nonlinear Fuzzy controller

Fuzzy control technique is often used in electrical drive control [103] but in power supply control it appears very seldom. A fuzzy solution is presented in [105] but it is combining

the fuzzy method with the PI controller. Updating the control parameters based on fuzzy rules it results in a self-tuning PI controller. The present work will present an individual fuzzy controller for the lower bandwidth voltage loop.

Fuzzy controller is usually chosen when it is difficult make accurate mathematical model of the system and it is based on human heuristic observation. Based on a predefined look-up table the control does not need advanced calculations and can be applied to low cost microcontrollers. Though making the decisions based on the look-up tables is time consuming thus the advantage of it can be used in low bandwidth control loops.

The basic fuzzy control block is shown in Figure 3.25:

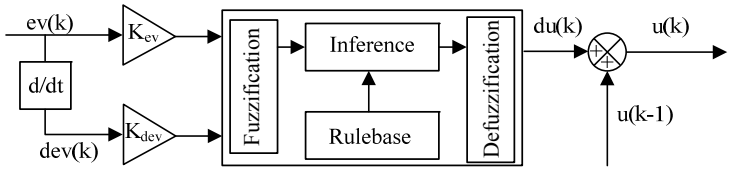


Figure 3.25: *Fuzzy incremental controller*

It is basically a closed loop decision maker, which compares the output value to a reference and determines the control signal to meet the performance requirements. The fuzzy block has four main components:

- Rulebase

  The *Rulesbase* consist of a set of rules, in form of logical statements (*If...then...*) which defines the way the controller should work.

- Inference

  The $Inference$ checks which rules are relevant at the respective control sequence and determines which control signal should be given to the system.

- Fuzification

  The $Fuzzification$ defines the input signals as they can be interpreted by the *Rulebase*.

- Defuzzification

  The $Defuzzification$ converts the results of the $Inference$ into values corresponding to the input of the controlled system.

The output of the fuzzy control block is added to the value obtained from the previous control sequence thus realizing an incremental controller (similar to a PI controller). The two input gains also show similarities to the PI controller parameters. To design a fuzzy controller a specific amount of knowledge should be accumulated about the system behavior based on observation. These informations has to be quantified in order to be processed by the control environment (computer, microprocessor).

Each input information belongs to one or two so called $membership\ functions$. These membership functions (μ) have a peak point where the $\mu(< input >) = 1$. For different

inputs they can take values between 0 and 1 and this shows that the specific input in which percentage belongs to the given membership function. Different *membership functions* exist: triangular, trapezoidal, Gaussian. A set of $\mu(< input >)$ numbers belonging to one membership function is called *fuzzy set*. Usually a two-input fuzzy control system is used (error and error variation as inputs). In a two dimensional *Rulebase* table usually four values are active as one input can only belong to maximum two membership functions in a percentage bigger than 0. This makes calculations even easier while writing the control firmware.

These values are processed by the *Inference* based on the *Rule base* criterion. If the *Rulebase* connects the two inputs with AND then the $\min(\mu(< input1 >), \mu(< input2 >))$ is the result. If the connection is with OR then the $\max(\mu(< input1 >), \mu(< input2 >))$ is considered. The result is a weighting table containing numbers which represent the belonging percentage of the inputs to the specific membership functions.

The standard fuzzy system uses singleton output membership functions (also called zero order Sugeno fuzzy system). Considering the defuzzification method, different methods are described in the literature [101]-[106]. The center-average defuzzification method is mostly used in control applications as it consists of a multiplication of the weighting table with the output zero order singleton values and division of the result by the sum of the weighting table elements.

A concrete example how fuzzy controller works can be found later in Section 4.2.2.5.

When using fuzzy controller beside advantages like no modeling needed and, easy to design and implement based on the measured values only and using human heuristic knowledge also there are some disadvantages. Is the human observer able to cover all the possible situation and predict the system behavior and implement stability criteria (overshoot, rise time, settling time)? These things have to be investigated and compared to the conventional controller parameters, which can be determined in a well defined way.

The main application area of fuzzy controllers are: low dynamic process control systems (temperature in heating chambers, level in water- or pressure in gas tanks), motor control (speed and position), robotics and autonomous vehicles. In power electronics, especially in switched mode power supply industry the calculation time of the fuzzy controller might be limited by the high switching frequency and high controller bandwidth requirements.

3.4 Summary

Different challenges and requirements were presented in this chapter in order to design a digital controller. Firstly different challenges like sampling and PWM resolution, aliasing effect and proper bandwidth selection are discussed. Afterwards the small signal model of the boost, interleaved boost and PSFB converters is built, the required transfer functions are obtained and discretization is performed with the most suitable method. The most commonly used controller in power electronics is the PI controller. Digital implementation of it is discussed. Thanks to the digital solution an alternative to the PI controller, a nonlinear solution can be applied. The fuzzy control method is introduced and discussed as high frequency voltage control solution.

Chapter 4

Digital control in application

This chapter will present two case studies applying digital control for switch-mode power-supplies. The first one is a 70W two-stage PFC/DC-DC converter using simple boost for PFC and RCD-clamped forward converter, controlled by a dsPIC30F1010 microcontroller. The hardware and performance comparison of digitally controlled and analog controlled two identical converters is presented. The second converter is also a two-stage 600W PFC/DC-DC converter using interleaved boost power factor corrector and phase-shifted full-bridge converter with synchronous rectification and current doubler to meet load demands. It is controlled with a single dsPIC33FJ32GS406. The use of fuzzy logic for voltage control is proposed and presented.

To prove the applicability of the digital control and confirm the hypothesis of the research, that digital control is feasible for high frequency switched-mode power supplies, different converters were built and control algorithms were implemented in digital microprocessors. The following chapter presents a set of case studies on different converter topologies for different power levels.

The main target of the investigation is to identify the compromises in cost effective and high efficiency converter design with embedded digital controller. To reduce manufacturing costs it is necessary to investigate the design of magnetic components in order to reduce the size and complexity. This might introduce in the design additional passive and active components, fact penalized in efficiency. Leading towards digital control in switched-mode power supply industry, the hardware design has to consider controllability with digital signal processors and all the additional circuitry required for data collection. Considering all these issues a low power and a middle power level power factor corrector and DC-DC converter was designed, built, tested and analyzed.

4.1 70 W two-stage PFC/DC-DC power supply

Firstly a low power solution was chosen to be implemented in order to test the control strategy and the power converter design. A 70W two-stage converter was designed, built and control strategy implemented in a dsPIC30F1010 microcontroller. The following case study had three steps: Firstly the converter was designed and built on a separate PCB and controlled with a 16-Bit 28-Pin Starter Development Board from Microchip using the

earlier mentioned dsPIC (Figure 4.1 and 4.2).

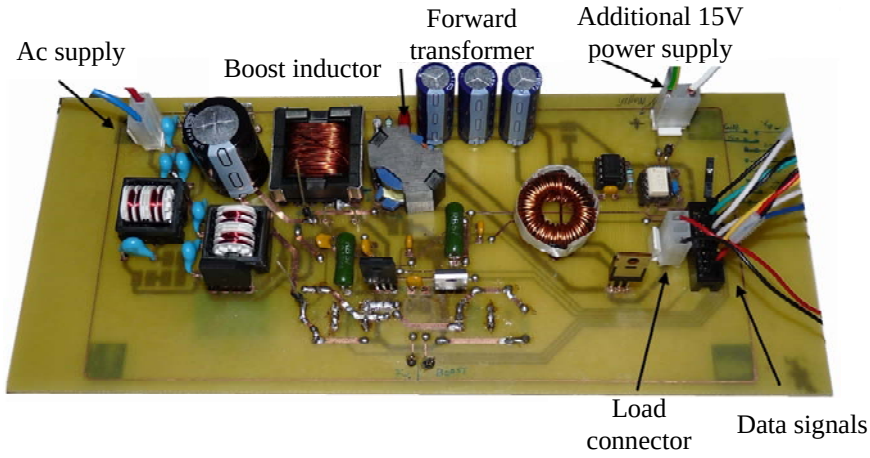


Figure 4.1: *First prototype*

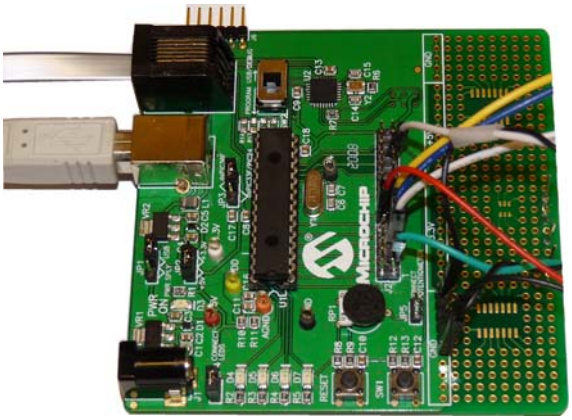


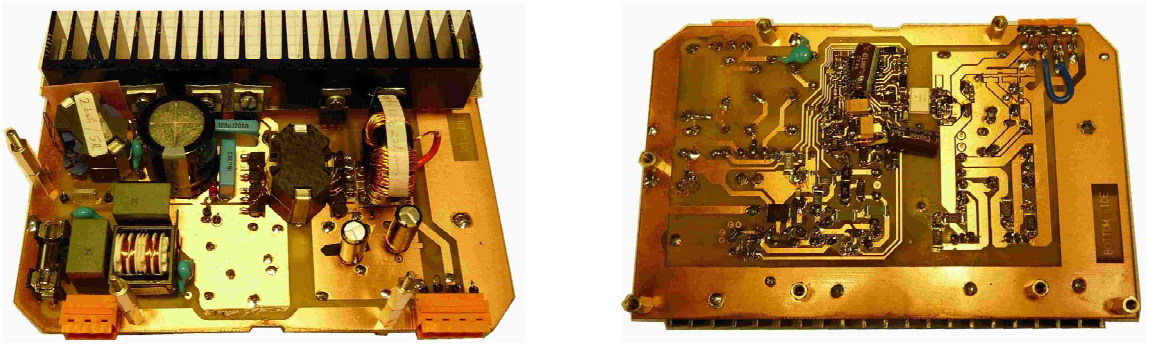
Figure 4.2: *16 bit 28 pin control board*

After some partial results, the converter layout was redesigned to reduce the noise sensitivity and also the microcontroller was embedded to the power board (Figure 4.3).

a.) b.)

Figure 4.3: *Power supply with digital controller*

To make a validation of the results obtained from the digitally controlled solution, the same converter was built using state-of-art UCC28510 analog controller, available in on the market (Figure 4.4).



a.) b.)

Figure 4.4: *Power supply with analog controller*

4.1.1 Converter description

The system consists of a non-isolated power factor corrector and an isolated DC-DC converter built up in cascade configuration. Choosing the two converters was driven by the idea of what topologies are commonly used in power supply applications with the traditional analog controllers. Thus for low power application a simple boost converter has the role of power factor corrector and a forward converter with RCD snubber ensures isolation between the load and the grid and meets the required load conditions. The boost converter from its natural characteristics provides good control over the line current waveform and has capacitive energy storage. As disadvantage it can be mentioned the lack of switch between the line and output. Thus it needs higher precaution regarding inrush, over current and over voltage protection. As the output voltage of the boost converter is higher than the peak input voltage, a second stage is required to meet load requirements.

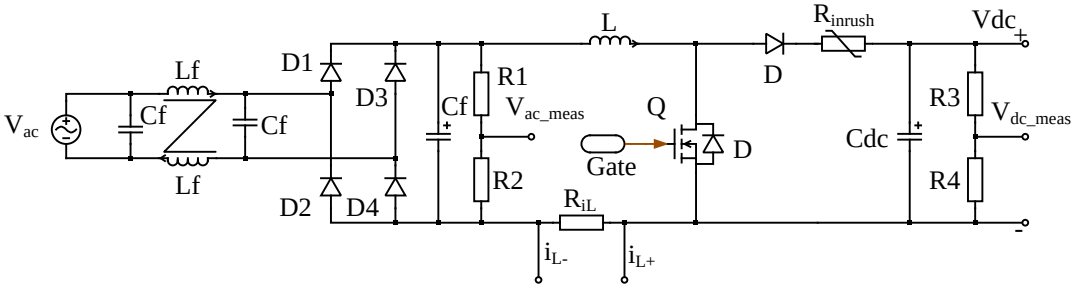


Figure 4.5: *Boost converter schematic*

As a second stage a forward converter with RCD snubber was chosen to reduce the output voltage and provide isolation. This topology is little different from the classical forward converter. The transformer demagnetization is solved by an RC snubber connected with a diode to the primary side of the transformer. Snubber losses might decrease

efficiency but manufacturing the simple high frequency forward transformer without additional winding will compensate in size and cost.

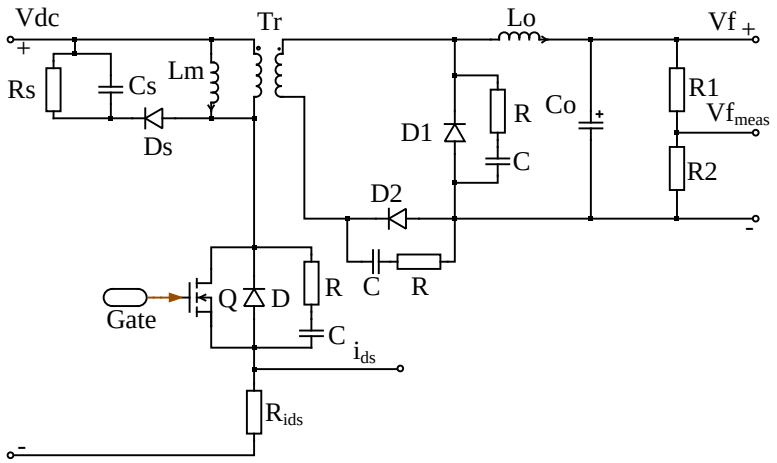


Figure 4.6: *Forward converter schematic*

Designing the components for the converters has to take into considerations the main goals presented in the introduction of this Chapter. To reduce the size of the magnetics, the design focused on operating the inductors in continuous conduction mode (CCM). Thus the RMS and peak currents are smaller in CCM than in DCM reducing copper and conduction losses. In CCM the small signal analysis of the converter is much easier than in DCM where the conversion ratio is load dependent [10]

In boost converter design one of the key components is the boost inductor. It was designed for universal input voltage and line frequency. The nominal output power is defined as Po=70 W with the desired efficiency of η=95%. The switching frequency f_s was set to 100 kHz and the inductor windings were placed inside an N87 type Siferrite core with RM10 shape.

Boost PFC design parameters	
V_{ac}	85-265 V
Vdc	400 V
Po	70 W
η	92%
f_L	40-60 Hz
f_s	100 kHz
ΔI	$25\% \cdot I_{Peak}$ - peak-to-average ripple

The above design parameters lead to the inductor value of L=2.7 mH, calculated with [81]:

$$L = \frac{(Vdc - V_{ac-min}) \cdot \frac{V_{ac-min}}{Vdc}}{2 \cdot \Delta I \cdot f_s} \tag{4.1}$$

where Vdc is the output voltage, V_{ac-min} is the minimum input voltage, ΔI is the inductor current ripple and f_s is the switching frequency. As the output voltage Vdc is 400 V the boost transistor and diode were rated to 600V. To reach a compromise between the reduced

output voltage ripple, the capacitor size and dynamic behavior of the system a Cdc=120 μF was chosen as capacitive energy storage. A 15 Ω thermistor limits the inrush charging current of the capacitor at startup (Figure 4.5) (design in A.1) As the input voltage is a rectified sinusoidal voltage, the duty cycle, peak current and current ripple are varying according to the input voltage. Figure 4.7 shows these values for 230 V_{RMS} operation.

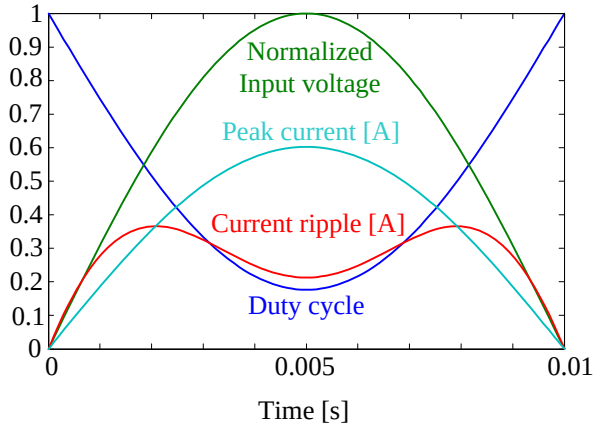


Figure 4.7: *Inductor current and duty cycle variation*

In the forward converter design also reducing the size and complexity of the magnetic components was the goal. Thus a simple high frequency (100 kHz) transformer was designed to generate the required output voltage and current.

Forward DC-DC design parameters	
Vdc	400 V
Po	70 W
η	92%
Vf	2x14 V
f_s	100 kHz
D	30%

Based on design requirements the transformer was designed with $\frac{N_s}{N_p} = \frac{1}{8}$, where N_p is the number of turns in the primary and N_s is the number of turns in the secondary winding. As the converter has two outputs, two secondary windings were designed. The transformer windings are place in an RM10 core just as the boost inductor. Instead of using an additional winding, for transformer reset a low cost and flexible solution was implemented in form of an RCD snubber. Although the reset circuit dissipates a part of the magnetizing and leakage energy, it limits the the peak value of the clamping voltage, set by the clamping resistor Rs [107] . Thus the rating of the switching MOSFET can be reduced to close to twice the input voltage. The magnetizing inductance of the transformer was set to Lm=17 mH and the duty cycle maximized to $D = 30\%$. With lower duty ratio higher efficiency can be achieved while using RDC reset circuit [107] (design in A.2).

To reduce the number of magnetic components, the two windings of the output filter inductors were coupled on a single Kool Mu material toroid core. The output filter

inductance value can be defined as [81]:

$$Lo = \frac{(Vf + V_D) \cdot (1 - D)}{2 \cdot \Delta I \cdot f_s} \tag{4.2}$$

where V_D is the voltage drop on the rectifier diodes and ΔI=$0.2 \cdot \frac{Po}{Vf} = 1A$ is the peak-to-average ripple. Thus the inductance value was defined to be Lo=100 μH each. For reducing the voltage ripple on the output, the filter capacitors were chosen to have a total value of Co=1200 μF on each output.

4.1.2 Controller design and description

Average current mode control was chosen to be implemented for the boost converter. In digital signal processors the average current value is sampled and processed during one switching period. Thus this control strategy is suitable for programming the control algorithm. To make proper controller design, firstly the converter small signal model has to be developed. Introducing the design parameters in the model developed in Section 3.2.1 the transfer functions of the system can be determined. As the transfer functions are load dependent (R), the converter stability was analyzed from light load to nominal load conditions and controller was designed for nominal load.

4.1.2.1 Boost inductor current control

Firstly the internal current loop design is presented. The current is measured with a resistor ($R_{iL} = 0.12\Omega$) as shown in Figure 4.5. The measured signal is amplified with 26 dB in a INA193 differential amplifier (Appendix B.3), thus scaled to the voltage level of the analog-digital converter. This is all can be included in the model duty cycle-to-inductor current transfer function gain G_{id0} shown in the Section 3.2.1.3:

$$\begin{aligned} G_{id0} &= \frac{2 \cdot Vdc}{D^2 \cdot R} \cdot R_{iL} \cdot G_{INA193} \\ D &= 1 - \frac{V_{ac-min}}{Vdc} \\ D' &= 1 - D; \end{aligned} \tag{4.3}$$

where R represents the load resistance and $G_{INA193} = 20$ is the voltage amplification of the differential amplifier and D is the duty cycle according to the rectified line voltage. The duty cycle-to-inductor current transfer function derived in 4.4 is a second order system, with one zero:

$$G_{id}(s) = G_{id0} \cdot \frac{\frac{R \cdot C}{2} \cdot s + 1}{\frac{L \cdot C \cdot s^2}{D^2} + \frac{L \cdot s}{D^2 \cdot R} + 1} \tag{4.4}$$

The above equation can modified and written in the general form of the second order

system:

$$G_{id}(s) = G_{id0} \cdot \frac{\omega_n^2 \cdot (\frac{1}{\omega_{iz}} \cdot s + 1)}{s^2 + 2 \cdot \zeta \cdot \omega_n \cdot s + \omega_n^2} \text{ ,where} \tag{4.5}$$

$$\omega_n = \sqrt{\frac{D^2}{L \cdot C}} = 1.446 \cdot 10^3 \text{ rad/s} \tag{4.6}$$

$$2 \cdot \zeta \cdot \omega_n = \frac{1}{R \cdot C} = 3.788 \tag{4.7}$$

$$\omega_{iz} = \frac{2}{C \cdot R} = 7.57 \text{ rad/s} \tag{4.8}$$

$$G_{id0} = 1.27 \tag{4.9}$$

The ω_n is the undamped natural frequency and ζ is the damping ratio.

Thus the plant's duty cycle-to-inductor current transfer function looks like:

$$G_{id}(s) = 1.27 \cdot \frac{2.09 \cdot 10^6 \cdot (0.1321 \cdot s + 1)}{s^2 + 0.258 \cdot s + 2.09 \cdot 10^6} \tag{4.10}$$

As the switching frequency was set to 100 kHz, the current signal is sampled with 50 kHz. In such way every second pulse generates a sampling sequence. This frequency is high enough to estimate the average value of the inductor current with high accuracy. This being decided, the continuous frequency domain model has to be discretized with the same time step, as the real microcontroller does it. So the sampling time for the current loop has been defined as $T_{si} = 20\mu s$. The discrete duty cycle-to-inductor current transfer function is obtained using the *Bilinear transformation* discretization method, presented in Section 3.2.4. The respective Matlab command is:

$$G_{id}(z) = c2d(G_{id}(s), T_{si}, 'tustin');$$

$$G_{id}(z) = \frac{3.511 \cdot z^2 + 0.5319 \cdot 10^{-3} \cdot z - 3.51}{z^2 - 1.999 \cdot z + 0.9999} \tag{4.11}$$

With the discrete transfer function the discrete controller can be designed. The goal is to obtain a controlled system with a closed loop bandwidth of close to 10 kHz. This means that the closed loop gain should cross the -3 dB level close to 10 kHz.

Design requirements are:

- The maximum overshoot, which is equal to the maximum deviation of the step response of the system from the reference value should be smaller than 5%.

$$M_p \approx e^{-\frac{\pi \cdot \zeta}{\sqrt{1-\zeta^2}}} \approx 0.05$$

As it is dependent on the damping factor, this can be calculated back as:

$$\zeta = \frac{|ln(M_p)|}{\sqrt{\pi^2 - ln(M_p)^2}} \approx 0.69$$

- At the frequency ω_i where the phase of the open loop system crosses the $-180°$, the gain should be positive in dB:

$$\begin{aligned} Gm &= \frac{1}{|G(j\omega_i)|} \\ Gm \text{ dB } &= 20logGm = -20log|G(j\omega_i)| \end{aligned} \tag{4.12}$$

  where Gm is the gain margin.

- At the open loop cutting frequency where the gain crosses the 0 dB, the phase margin should be higher than 60°.

$$Pm = 180° + \phi$$

  where Pm is the phase margin and ϕ is equal to the phase in degree at cutting frequency.

To control the inductor current, a classical PI controller is used (Figure 4.8). The controller transfer functions in the continuous and discrete domain was shown in equations 3.97-3.98. Even though it has more than two stable poles, the controlled open loop system can be treated as a second order system because the stability is influenced only by the dominant poles. The dominant poles are the ones placed the closest to the $z = 1$ in the discrete domain.

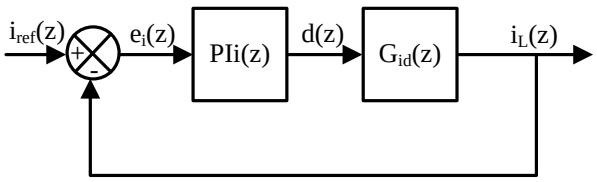


Figure 4.8: *Current loop*

Using the earlier defined design parameters and the discrete duty cycle-to-inductor current transfer function and discrete PI transfer function, the *Matlab SISOTOOL* toolbox was used to determine the Kpi and Kii values. The root-locus of open loop system was drawn and the controller parameters were adjusted such that the closed loop system has the required damping and crossover frequency with the desired phase margin. Thus:

$$\begin{aligned} Kpi &= 0.21 \\ Kii &= 0.07032 \end{aligned}$$

The root-locus and the open loop bode plot with the phase and gain margins of the controlled system is shown in Figure 4.9-4.10. Figure 4.9 shows the system response with

the set controller parameters in case of light load conditions. The damping factor and undamped natural frequency lines are shown in the figure.

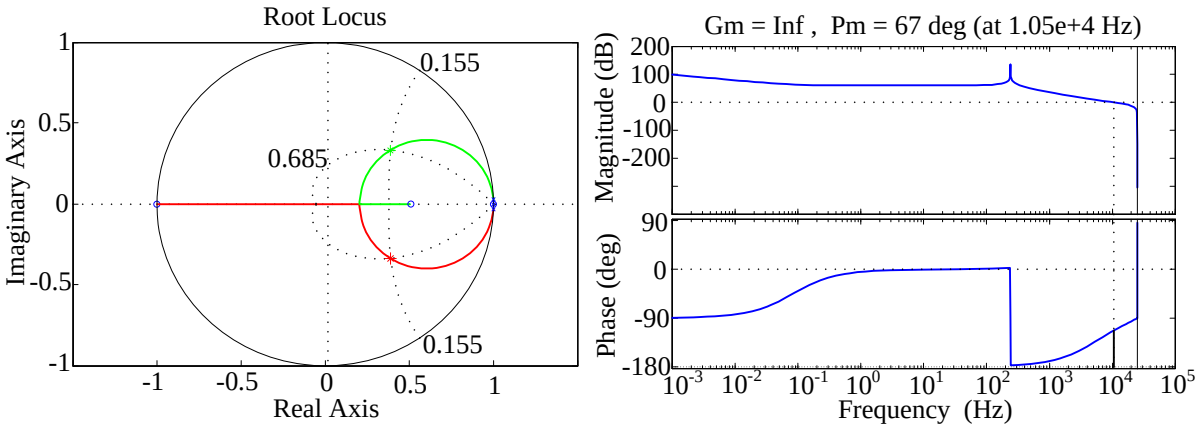


Figure 4.9: *Current controller design light load*

The closed loop poles are:

$$\begin{aligned} &0.9998; \\ &0.3793 + 0.3360j; \\ &0.3793 - 0.3360j; \end{aligned}$$

The system has the damping factor and undamped natural frequency of:

$$\zeta = 0.685 \tag{4.13}$$

and the gain and phase margins:

$$\begin{aligned} Pm &= 67^\circ \text{ at } 10.5 \text{ kHz} \\ Gm &= Inf \end{aligned}$$

Figure 4.10 present the system behavior with full load.

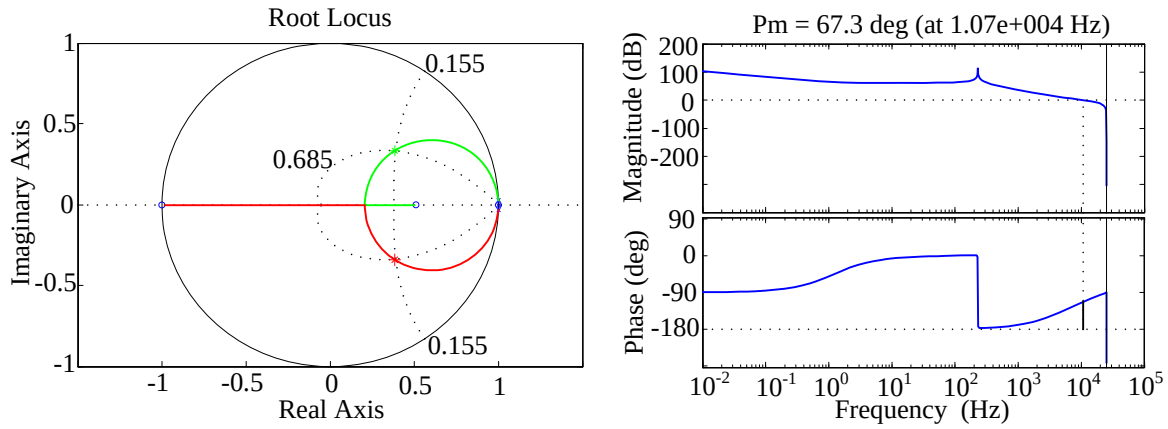


Figure 4.10: *Current controller design for full load*

The closed loop poles are:

$$\begin{aligned} 0.9998; \\ 0.3794 + 0.3361j; \\ 0.3794 - 0.3361j; \end{aligned}$$

In this case the system has the damping factor and undamped natural frequency of:

$$\zeta = 0.685 \tag{4.14}$$

and the gain and phase margins:

$$\begin{aligned} Pm &= 67.3^{\circ} \text{ at } 10.7 \text{ kHz} \\ Gm &= Inf \end{aligned}$$

All the closed loop poles are within the unity radius circle. The gain and phase margins are within the requirements. These results show that the designed controller is able to stabilize the current loop from light to full load.

4.1.2.2 Boost output voltage control

The boost voltage loop is the external loop with lower dynamics. The bandwidth is usually set to be less than the normal frequencies present in the controlled system. As the output voltage has a ripple of 100 Hz due to the rectified line voltage, the bandwidth of the voltage controller was required to be around 10 Hz.

The calculations start with determining the duty cycle-to-output voltage transfer function: G_{vd}. The output voltage is measured with a voltage divider (Figure 4.5 - V_{dc_meas}) and the measured value is scaled to ADC voltage level with an INA193 differential amplifier.

The gain of the transfer functions is:

$$G_{vd0} = \frac{Vdc}{D'} \cdot R_{div} \cdot G_{INA193} = 4.794$$
$$R_{div} = \frac{R_3 \cdot R_4}{R_3 + R_4} = 0.5 \cdot 10^{-3}$$
$$G_{INA193} = 20;$$

The duty cycle-to-output voltage is similarly a second order system, and with small modifications it can be written in form of the classical second order system. It has a positive zero at $s = 5.525 \cdot 10^5$.

$$G_{vd}(s) = G_{vd0} \cdot \frac{\omega_n^2 \cdot (-\frac{1}{\omega_{vz}} \cdot s + 1)}{s^2 + 2 \cdot \zeta \cdot \omega_n \cdot s + \omega_n^2} \text{ ,where} \tag{4.15}$$

$$\omega_n = \sqrt{\frac{D'^2}{L \cdot C}} = 1.446 \cdot 10^3 \text{ rad/s} \tag{4.16}$$

$$2 \cdot \zeta \cdot \omega_n = \frac{1}{R \cdot C} = 3.788 \tag{4.17}$$

$$\omega_{vz} = \frac{D'^2 \cdot R}{L} = 5.525 \cdot 10^5 \text{ rad/s} \tag{4.18}$$

$$\tag{4.19}$$

The sampling frequency of the output voltage is 5 times smaller than the one of the current. Thus the discrete mode uses a $T_{sv} = 100\mu s$ as sampling time. By using the following Matlab command, the discrete $G_{vd}(z)$ transfer function can be obtained.

$$G_{vd}(z) = c2d(G_{vd}(s), T_{sv}, 'tustin');$$

$$G_{vd}(z) = \frac{0.024 \cdot z^2 + 0.05 \cdot 10^{-3} \cdot z + 0.0258}{z^2 - 1.979 \cdot z + 0.9996} \tag{4.20}$$

The transfer function of the voltage control loop can be derived from the duty cycle-to-output voltage, duty cycle-to-inductor current and the current PI controller as shown in Figure 4.11.

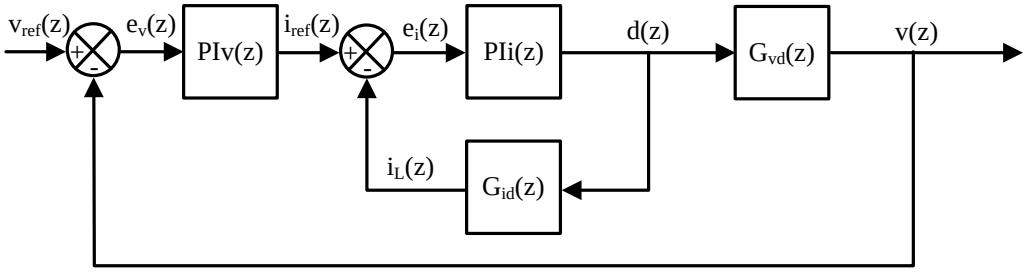


Figure 4.11: *Voltage loop*

Before determining the voltage controller parameters, the discrete G_{vd} has to be combined with the closed current loop.

$$G_{sysv}(z) = \frac{PIi(z)}{1 + PIi(z) \cdot G_{id}(z)} \cdot G_{vd}(z) \tag{4.21}$$

The resulting combined transfer function is:

$$G_{sysv}(z) = \frac{1.249 \cdot 10^{-3} \cdot z^3 + 2.9 \cdot 10^{-3} \cdot z^2 + 1.99 \cdot 10^{-3} \cdot z + 0.33 \cdot 10^{-3}}{z^3 - 0.046 \cdot z^2 - 0.6311 \cdot z - 0.3211} \tag{4.22}$$

To control the output voltage the same PI controller transfer function is used as defined in 3.98, where $T_s = T_{sv}$. Similarly to the current controller, the design requirements are:

- The maximum overshoot, which is equal to the maximum deviation of the step response of the system from the reference value should be smaller than 2.5%.

  $$M_p \approx 0.025$$

  thus the damping factor should be:

  $$\zeta \approx 0.76$$

- At the frequency ω_i where the phase of the open loop system crosses the $-180°$, the gain margin should be positive in dB.

- At the open loop cutting frequency where the gain crosses the 0 dB, the phase margin should be higher than 60°.

Similarly, to make the voltage controller design, *Matlab SISOTOOL* toolbox was used to determine the Kpv and Kiv values. The root-locus of open loop system was drawn and the controller parameters were adjusted such that the closed loop system has the required damping and crossover frequency with the desired phase margin. Thus:

$$Kpv = 0.99998$$
$$Kiv = 0.00125$$

The root-locus and the open loop bode plot with the phase and gain margins of the controlled system is shown in Figure 4.12-4.13. Figure 4.12 shows the system response with the set controller parameters in case of light load conditions.

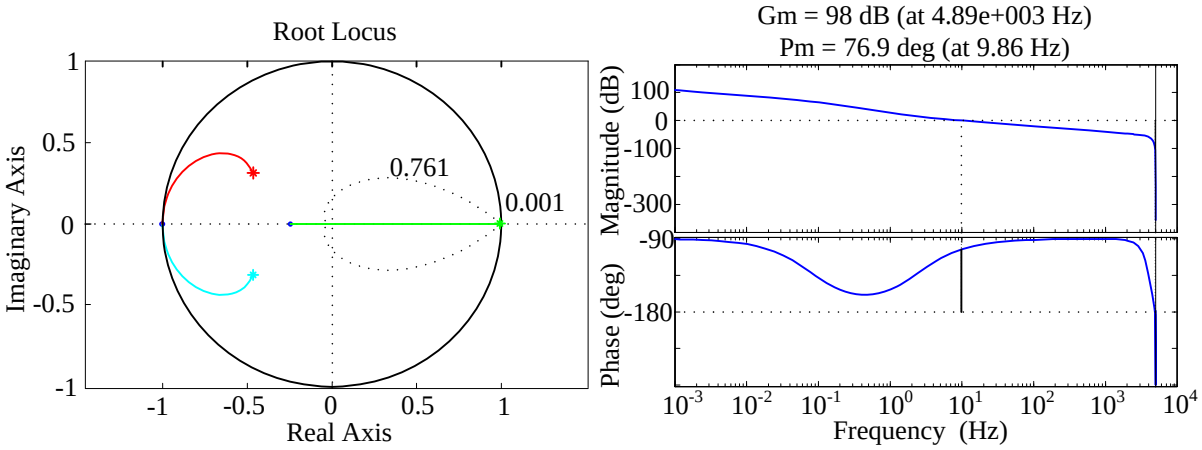


Figure 4.12: *Voltage controller design for light load*

The closed loop poles of the voltage control system at light load are:

$$\begin{aligned} 9.9854e-1+1.2051e-3j \\ 9.9854e-1-1.2051e-3j \\ -0.4766e-1+0.3071j \\ -4.7664e-1-0.3071j \end{aligned}$$

The dominant poles are the first two being positioned closed to the $z = 1$. Their damping factor and the undamped natural frequency is:

$$\zeta = 0.769 \tag{4.23}$$

The cut-off frequency is 9.86 Hz, where the phase margin is:

$$\begin{aligned} Pm &= 76.9^{\circ} \\ Gm &= 98 \text{ dB at } 4890Hz \end{aligned}$$

Figure 4.13 present the voltage loop behavior with full load.

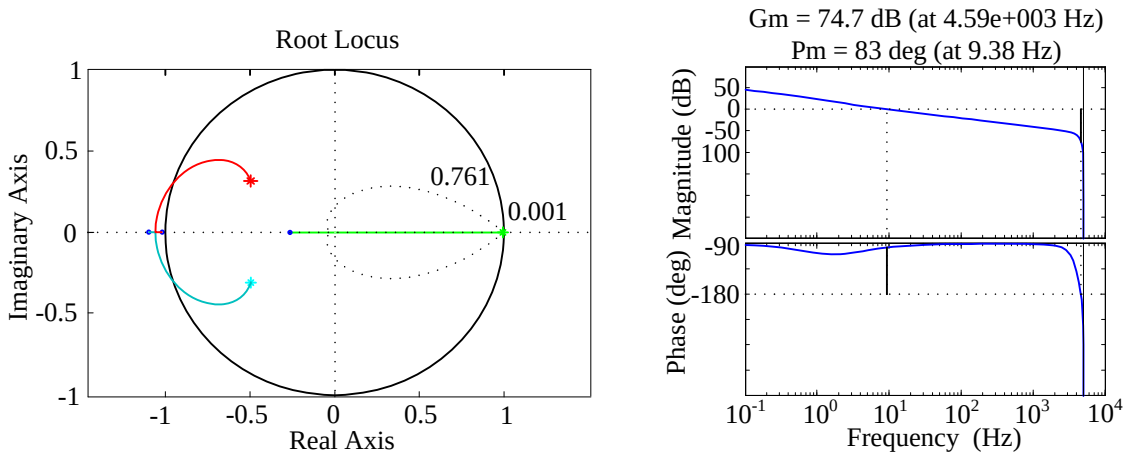


Figure 4.13: *Voltage controller design for full load*

The closed loop poles of the voltage control system at full load are:

$$\begin{aligned} 9.9819e-1+5.5314e-4j \\ 9.9819e-1-5.5314e-4j \\ -4.7664e-1+3.0715e-1j \\ -4.7664e-1-3.0715e-1j \end{aligned}$$

The dominant poles are the first two and their damping factor and the undamped natural frequency is:

$$\zeta = 0.95 > 0.76 \tag{4.24}$$

The damping factor is higher than the required minimum for the 2,5% overshoot, thus better transients can be achieved. The cut-off frequency is 9.38 Hz, where the phase margin is:

$$\begin{aligned} Pm &= 83^\circ \\ Gm &= 74.7 \text{ dB at } 4590Hz \end{aligned}$$

The closed loop poles of the voltage loop are within the unity radius circle. The gain and phase margins are within the requirements. These results show that the design controller is able to stabilize the voltage loop from light to full load.

4.1.2.3 Forward converter voltage control

The second stage in the power transfer is the forward converter. The control of the forward converter is also based on the same control structure as presented in Figure 3.23.

The voltage control is done with an analog shunt regulator, a TL431 [108]. The output voltage of the forward converter is measured (Figure 4.6 - Vf_{meas}) with a voltage divider. As the measured voltage reaches the reference value of the TL431 (V_{ref}=2.5V), it starts

conducting, thus it provides current to the LED of the optocoupler through R_3. As the photo transistor of the optocoupler starts conducting, the output, which is the the control signal, will decrease. This signal is the reference for the peak current controller (Ext_ref). V_f+ and V_f- are the output of the forward converter, VDD is the supply voltage for the microcontroller and VEE is the primary ground (Figure 4.14).

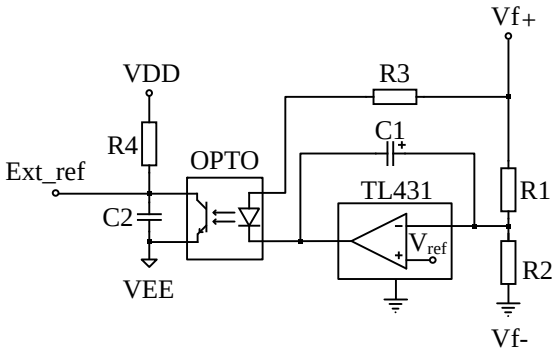


Figure 4.14: *TL431 voltage controller with optical isolation*

4.1.2.4 Forward converter peak current control

To limit the primary drain-source current (i_{ds}) of the forward converter, a peak current control solution was implemented, using the analog comparator module of the digital signal processor. The reference value is given by the voltage loop (Ext_ref) and it is compared to the measured current value. If the current is higher than the reference, the comparator module simply turns off the PWM pulse. As it has a fixed programmed duty cycle, in the next switching period the process starts from the beginning. Thus a duty cycle interval of [0 - 30%] can be achieved in function of the output voltage level.

4.1.3 Simulations

Matlab/Simulink environment was used to model the converter and the control algorithm (Figure 4.15). The large signal model of the boost converter was built in Matlab-embedded PLECS environment as shown in Figure 4.5. The measured signals ($V_{ac\_meas} = V_{ac}$, $V_{dc\_meas} = V_{dc}$, $i_{L+} = i_L$) are sampled and amplified in the same way as they would be done in the real application and used in the ADC interrupt (control algorithm).

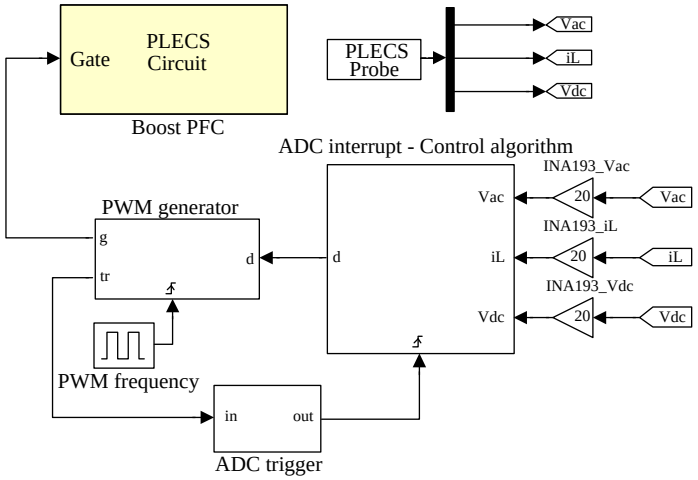


Figure 4.15: *Simulation block diagrams*

The *PWM generator* block is responsible for generating the switching pulses with the required duty cycle for the boost converter. Inside the block there is an embedded Matlab function, which generates a saw-tooth shape carrier wave, using a counter. It is compared to the input d, the duty cycle value to get the PWM pulses, g, and generates the tr, trigger pulse for the ADC interrupt. The switching frequency, as mentioned earlier it was defined as $F_s = 100$ kHz. The resolution of the PWM ramp is determined by the *PWM frequency* pulse generator. Due to simulation speed and time the PWM frequency generator was set to 10 MHz and the ramp counter saturation level to 99. The trigger signal is defined to be $tr = d/2$, as it is required to appear a trigger pulse in the middle of the ON state of the MOSFET. This trigger signal is also compared to the PWM ramp. As the *ADC Interrupt* block should be triggered in every second switching pulse, a frequency divider was introduces (Figure 4.16).

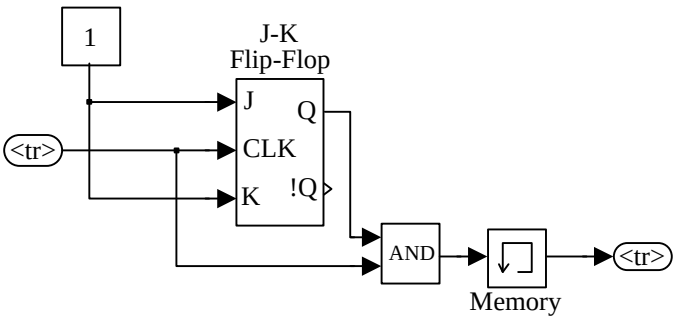


Figure 4.16: *ADC trigger - frequency divider*

The *ADC Interrupt* block is also an embedded Matlab's function. The code inside is similar to the C code programmed in the microcontroller. All the variables are transformed in $Q.15$ format and the operations are performed according to the Q.15 arithmetics. The obtained numbers are signed integers, represented on 16 bits. Such way a simulation platform very similar to the real life could be developed.

The interrupt consist of two parts:

- The inductor current, i_L and the input voltage, V_{ac} are sampled in every second switching sequence, with 50 kHz. The current reference i_{ref} is calculated by multiplying the actual output of the voltage controller (PIv) with the measured V_{ac}. The role of the input voltage is to provide a shape of the current reference. The current controller parameters, the proportional and the integrator part are also calculated simultaneously with the actual measured current error. The output of the current controller, the duty cycle is kept between [0-95%] of the switching period.

- The output voltage V_{dc_meas} is sampled and the voltage controller parameters are updated in every 10^{th} switching sequence. The output of the voltage controller is limited according to the required maximum current reference.

To transfer the measured values into signed integers the following formula is used:

$$X(Q.15) = x_{measured} \cdot ADC \cdot 32$$
$$ADC = \frac{1023}{4.2}$$

where $x_{measured}$ is a value between 0-4.2V and ADC is the analog-digital conversion factor in a 10bit ($'1032'$) scale with a reference voltage of $4.2V$. The term $'32'$ represents a 5 bit left shift from the lower 10 bit to the upper 11 bit of the 16-bit number, obtaining the signed Q.15 format.

Simulation results are presented in Figure 4.17 and Figure 4.18. Firstly line voltage harmonics were neglected. Figure 4.17 shows one line period of the inductor current, line current and normalized line voltage. The inductor current is maintaining the continuous conduction mode with an input line voltage of 230 V_{RMS}. Sinusoidal line current is achieved with low harmonic distortion. As the power supply was designed for intelligent light sources, it falls under the regulation of the standard EN 61000-3-2, group C. Figure 4.17 b.) compares the standard limitations (presented in Table 2.4). The THD of the line current was compared to the standard limitation values and instead of an admissible $St.THD = 0.33787$ the simulated value where $THD = 0.04351$. The power factor was calculated based on Section 2.2 and the result is $PF = 0.9801$.

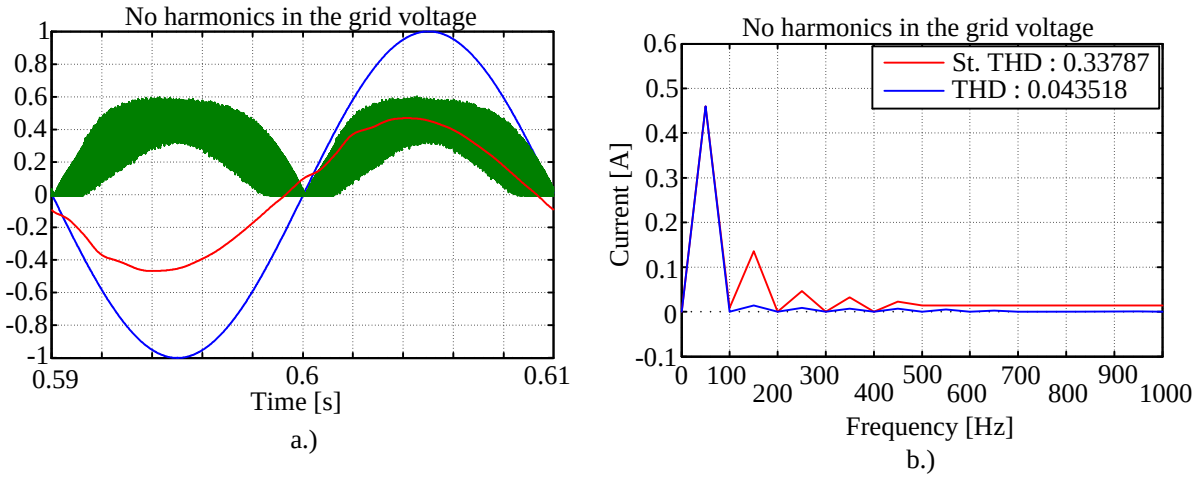


Figure 4.17: *Simulation results: a.) One line period - red: line current, green: boost inductor current, blue: normalized line voltage without voltage harmonics, b.) The current harmonic spectrum - red: Standard EN 61000-3-2, blue: simulated*

After adding harmonic components to the grid voltage, simulations were repeated and results are presented in the Figure 4.18. Harmonics were added to the line voltage based on the measured values in the Aalborg University laboratory, Denmark. The base frequency is $f_L = 50Hz$ and $V_{ac} = 230\ V_{RMS}$.

1^{st}	3^{th}	5^{th}	7^{th}	9^{th}	11^{th}
V_{ac}	0.35% of V_{ac}	1.13% of V_{ac}	0.77% of V_{ac}	0.12% of V_{ac}	0.17% of V_{ac}

Table 4.1: *Most significant harmonic components present in the line voltage*

With the introduced harmonics (Table 4.1), the line current harmonic distortion became $THD = 0.04295$ which is much below the limitations ($St.THD = 0.33541$). In this case the calculated power factor was $PF = 0.9706$.

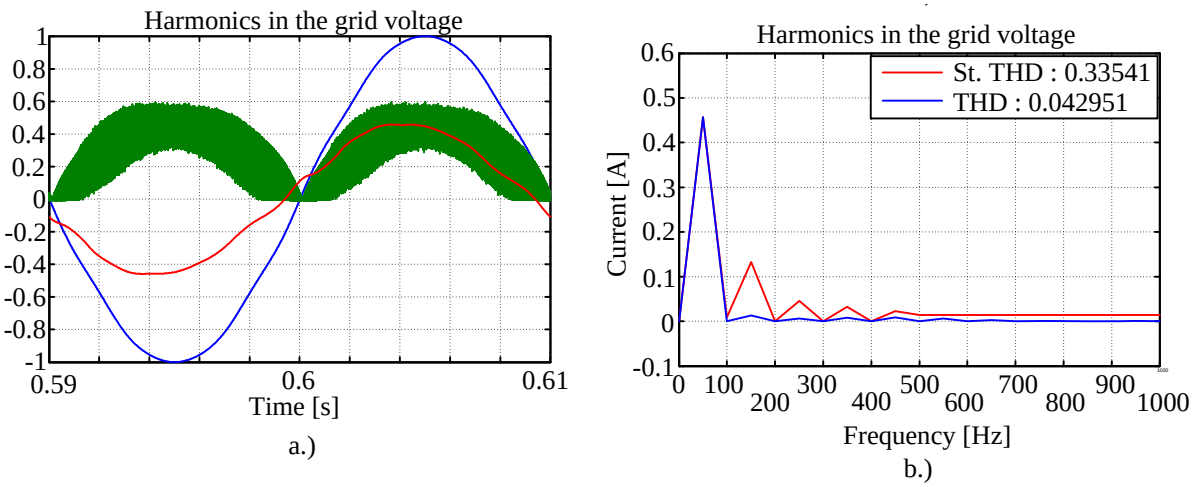


Figure 4.18: *Simulation results: a.) One line period - red: line current, green: boost inductor current, blue: normalized line voltage with voltage harmonics added, b.) The current harmonic spectrum - red: Standard EN 61000-3-2, blue: simulated*

4.1.4 Auxiliary power supply

External gate drivers are needed when using a digital signal processor. Also microcontroller has a very narrow supply voltage tolerance ($VDD = 3.5 - 5$ V). Thus it requires a stable supply voltage. To supply the dsPIC and the gate drivers, firstly two additional windings were designed for the forward transformer. This idea made the transformer design more complex and introduced problems at startup. While the transformer primary voltage was lower than nominal it could not provide power to the output and the dsPIC could not be started up.

Finally an additional small flyback converter was chosen (Figure B.4), connected to the DC link, to supply the dsPIC and the gate drivers (11-13 V). The converter at startup charges the boost capacitor. Reaching the minimum voltage level of $100V$ the flyback converter, controlled with a LinkSwitch LNK562 switch, turns on. The flyback transformer has two secondary windings, one is rated for 12 V output and the other one for 5 V. Only the 12 V output is controlled. This voltage is measured and fed back to the controlled switch. Such way a stable gate drive voltage and an uncontrolled dsPIC $VDD \approx 4.2$ V is obtained. This additional small supply converter introduce losses of 1.5-2 W.

4.1.5 Digital control implementation

From many fast digital controllers existing on the market a Microchip dsPIC30F1010 was selected to control the 70 W boost PFC and forward DC-DC converters.

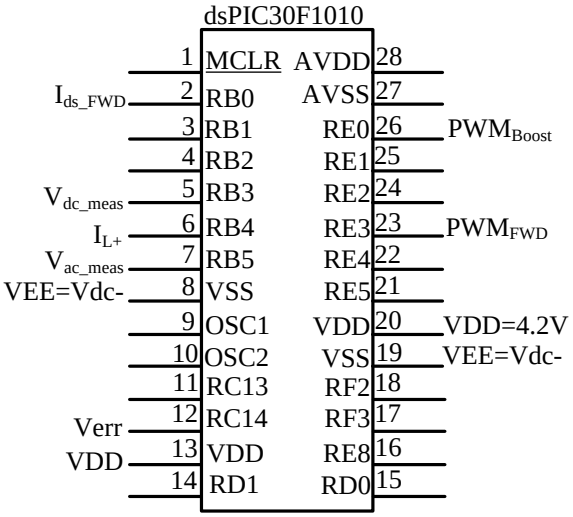


Figure 4.19: *dsPIC30F1010 microcontroller*

The 14.55 MHz fast internal RC oscillator with the 32X PLL and a division by 16 is able to generate an internal frequency of 29.1 MHz with basic settings. With tuning a maximum of 15 MHz internal frequency can be achieved. This means that one instruction time is 66.6 ns. The controller has fast PWM outputs with a PWM frequency generator of 465.6 MHz. To obtain a 100 kHz switching frequency a 13 bit PWM resolution and a saw tooth carrier waveform was used. Fast 10 bit analog-digital converters permitted current sampling frequency to be at 50 kHz. The average current mode control for the PFC converter programmed in Microchip Mplab code composer environment.

The dsPIC has a internal Analog Comparator module which was used to control the Forward converter. Peak current control was implemented for limiting the peak value of drain source current (i_{ds}) of the forward MOSFET. The converter was operated at 100 kHz switching frequency and a fixed duty cycle of 30%. During every switching sequence the comparator of the dsPIC compares the drain source current to the reference, Ext_ref, obtained from the secondary side voltage controller (Figure 4.14 - TL431) . If i_{ds_FWD} has greater value than the reference the comparator generates a fault signal which shuts down the PWM signal until the next switching period (Figure 4.20). Thus the peak current mode control is achieved.

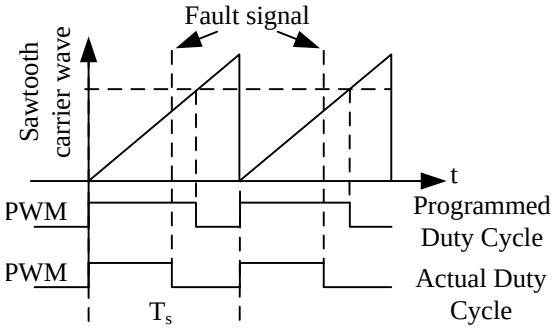


Figure 4.20: *Peak current control - PWM reset*

Firstly only the two-stage PFC and DC-DC converter was designed and built (Figure 4.1). Additional gate drive voltages were supplied by external power supply. The digital controller was also on a separate development board (Figure 4.2).

The first measurements were obtained with these boards and published in "Simple digital control of a two-stage PFC converter using dsPIC30F microprocessor" - PEMD 2010 - The 5th IET International Conference on Power Electronics, Machines and Drives - 2010, Brighton, United Kingdom.

At this early stage sinusoidal line current was generated with low harmonic distortion and high power factor (0.994) As it is visible in Figure 4.21 the inductor current is almost discontinuous during the whole half line period. This happened due to the too low boost inductance level (1.1 mH). High power factor can be explained with the discontinuous conduction mode. Also the first tests were done with a switching frequency of 50 kHz.

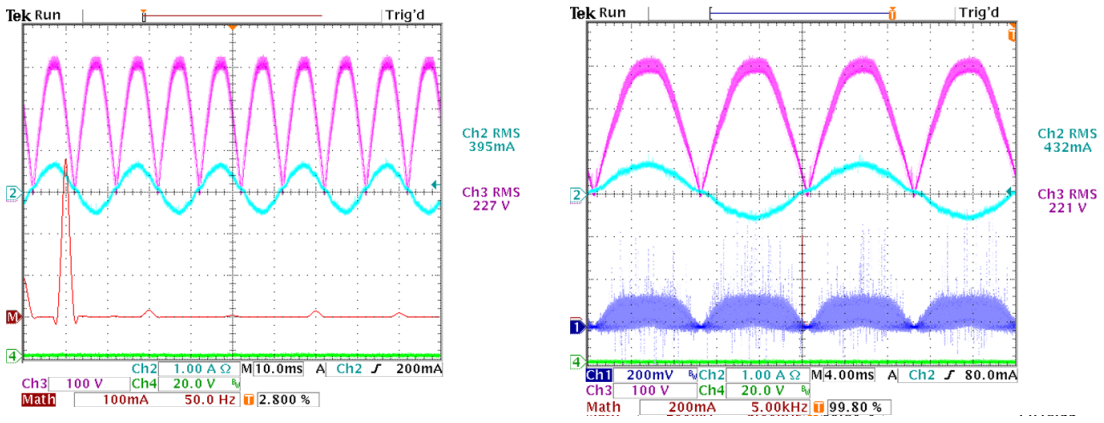


Figure 4.21: *First boost measurements - pink: rectified line voltage, cyan: line current, blue: inductor current, red: line current harmonics*

To optimize the performance and converter design, different operation frequencies were tested on the forward converter. As Figure 4.22 left picture shows, at lower switching frequency (50 kHz) the drain-source voltage of the forward MOSFET is increasing up to 1 kV. At 100 kHz this level is reduced to 740 V (Figure 4.22 right picture). To reduce the voltage stress on the switching transistor the 100 kHz operations frequency was selected for further investigation.

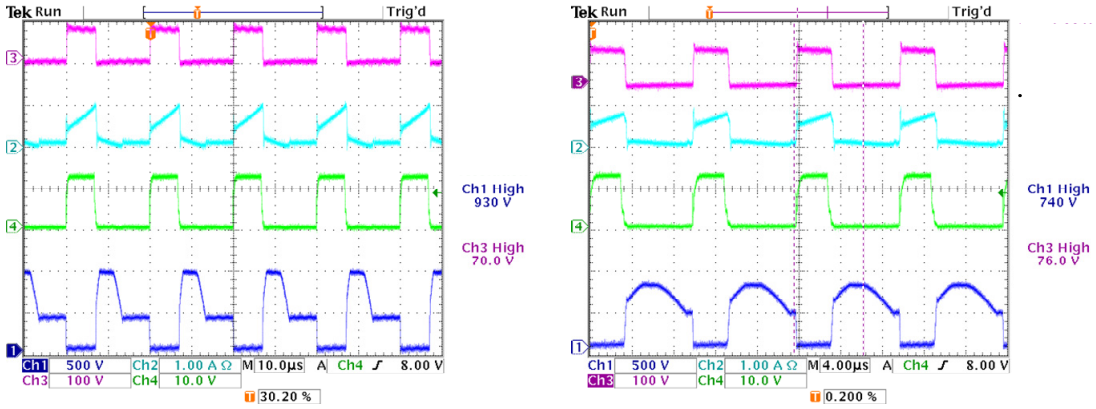
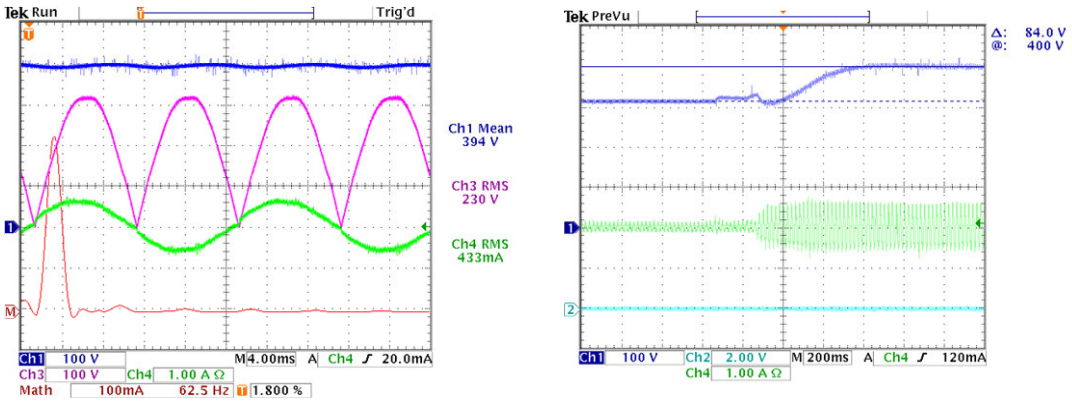


Figure 4.22: *First forward measurements - pink: rectified secondary voltage, cyan: forward MOSFET drain-source current, blue: drain-source voltage, green: gate signals*

Efficiency analysis at this level was not performed due to the fact that all the auxiliary voltages were taken from external supplies and the microcontroller was also placed on a separate board.

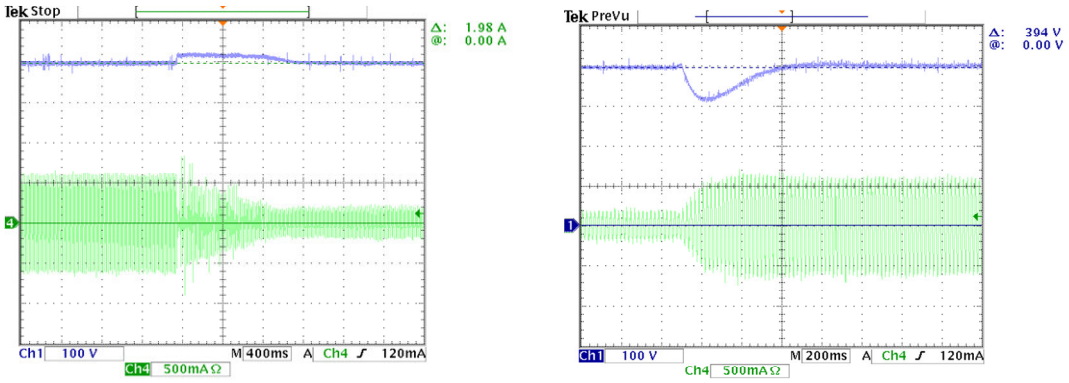
To eliminate the not desired noises, the layout of the converter PCB was redesigned and also the digital controller was embedded to the system. It was placed on the power board (Figure 4.3). As Figure 4.23 a.) shows, with this new design and embedded digital controller sinusoidal line current was achieved with a power factor of 0.97 and low current harmonic distortion (around 4% - measured with PM100 single phase power analyzer). These results validate simulation results, when line voltage harmonics were taken into consideration. The inductor was now rebuild to the designed value, presented earlier. Different operation conditions were tested. As Figure 4.23 b.) shows, the converter is started up like a normal rectifier without any switching. As the Vdc reaches the uncontrolled 300 V, the controller turns on and starts the control algorithm.



a.) b.)

Figure 4.23: *Boost converter waveforms a.) Green: line current, pink: rectified line voltage, blue: boost voltage, red: line current harmonics. b.) Startup condition (blue: boost voltage, green: line current)*

Load step tests were also performed. Figure 4.24 presents a load step from light to full load and from full to light load. In Figure 4.24 a.) it is visible that that an over voltage protection is implemented thus the boost voltage can not rise higher than 410 V.



a.) b.)

Figure 4.24: *Loadstep: a.) Full load to light load (green: line current, blue: Vdc boost voltage). b.) Light load to full load (green: line current, blue: Vdc boost voltage).*

Figure 4.25 shows the forward converter control signal ($Verr = Ext\_ref$) and according to this the MOSFET drain-source current (i_{ds}).

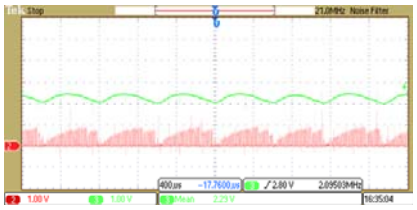


Figure 4.25: *Green: Forward converter control signal. Orange: Drain-source current*

4.1.6 Comparison of the digital controlled converter to and identical but analog controlled one

The digital control was implemented and embedded to the power supply. In order to validate its performance, another board was built, with the same design parameters and requirements. To control the second board, an analog controller from Texas Instrument, a UCC28510 combo PFC/PWM controller was chosen.

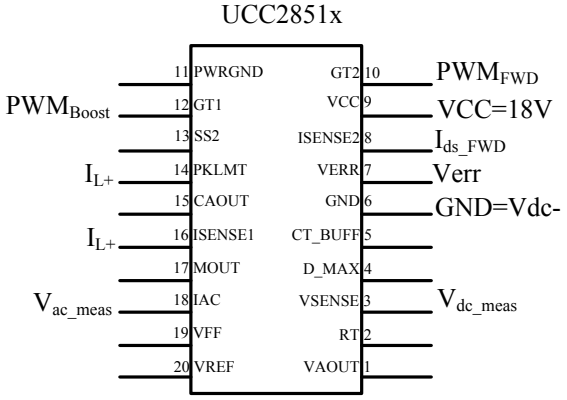
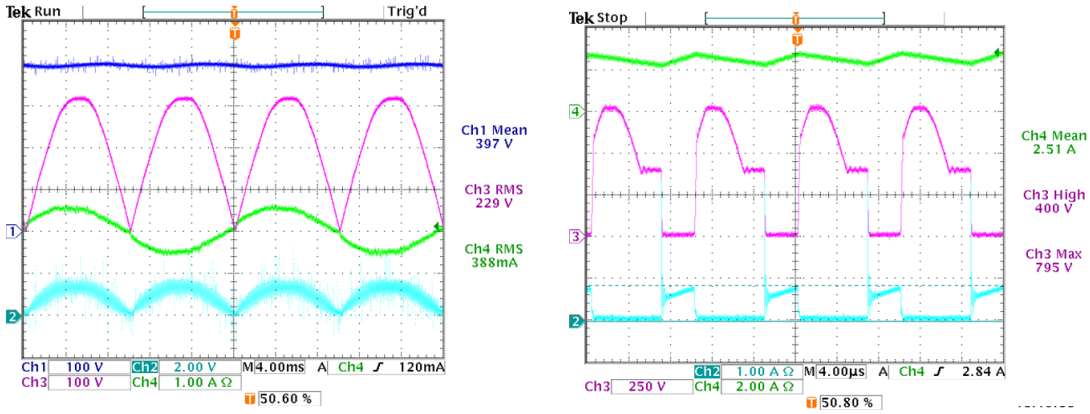


Figure 4.26: *Analog controller UCC28510*

In the analog controller also average current mode control is implemented for the boost converter and peak current control for the forward converter. This controller was chosen because both converters can be controlled by a single chip.

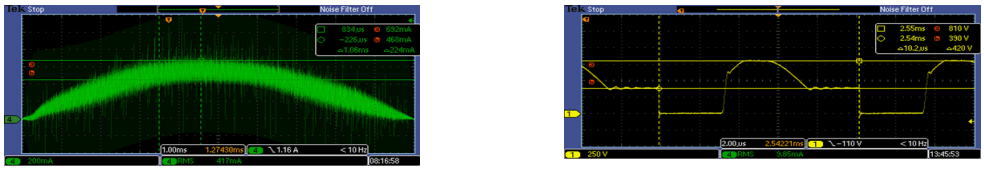
Just as in case of the digital controller, four signals had to be measured: V_{dc_meas}, $IL+$, V_{ac_meas}, ids and $Verr$. The DC-link voltage (Vdc_meas) gave the feedback for the PFC voltage control. The output of the voltage controller together with the measured rectified line voltage (Vac_meas) determined the reference for the current controller. The current controller compared the reference current with the measured average value of the boost inductor current (I_{L+}) and determined the duty cycle for the boost MOSFET. The peak current mode control of the second stage forward DC-DC converter was obtained by comparing the drain-source current of the Forward MOSFET (i_{ds_FWD}) with a voltage error signal ($Verr$). The $Verr = Ext\_ref$ is generated by the output voltage controller, a TL431 shunt regulator (Figure 4.14).

In the university laboratory the analog controlled converter was designed and built (Figure 4.4). Due to the structure of the controller, it has some small differences compared to the digitally controlled converter. The analog controller has integrated gate driver and needs a supply voltage of $VCC = 10 - 18$ V. This is obtained from an additional winding on the forward transformer. The mentioned voltage band shows flexibility and immunity to supply voltage variations. Additional startup circuit was required: a Supertex LR645 high voltage startup IC is used, which is turned off in steady state operation and the controller is supplied from the additional winding of the transformer. The introduced losses are around 0.9 W. Considering the price differences the UCC28510 was 11 DKK, the LR745 startup circuit was 3DKK, so the additional circuitry costs roughly 15 DKK. To this one could add the cost of adding one additional winding to the forward transformer. Meanwhile making calculations for the digital controller the dsPIC30F1010 was 20 DKK, the control Linkswitch for the additional small power supply 15 DKK, the flyback transformer 36 DKK and the combo gate driver 6 DKK. So the additional circuitry to supply the dsPIC cost around 80 DKK. The forward transformer was on the other hand an ordinary two winding high frequency transformer.



a.) b.)

Figure 4.27: *a.) Boost converter waveforms b.) Forward converter waveforms*



a.) b.)

Figure 4.28: *a.) Boost inductor current b.) Forward drain source voltage*

In Figure 4.28 a.) the continuous conduction mode of the Boost inductor is shown for the analog controller. Figure 4.27 a.) presents the voltage and current waveforms for the digital controller. Figure 4.28 b.) and Figure 4.27 b.) show the Forward converter waveforms: drain source voltage in case of analog control (Figure 4.28 b.)) and drain-source voltage, current and output inductor current for digital control (Figure 4.27 b.)) respectively. Figure 4.29 show the efficiency and power factor curves for the two converters. At light load conditions the power factor is higher in case of digital control but the use of additional power supply and modify transformer design is punished in efficiency.

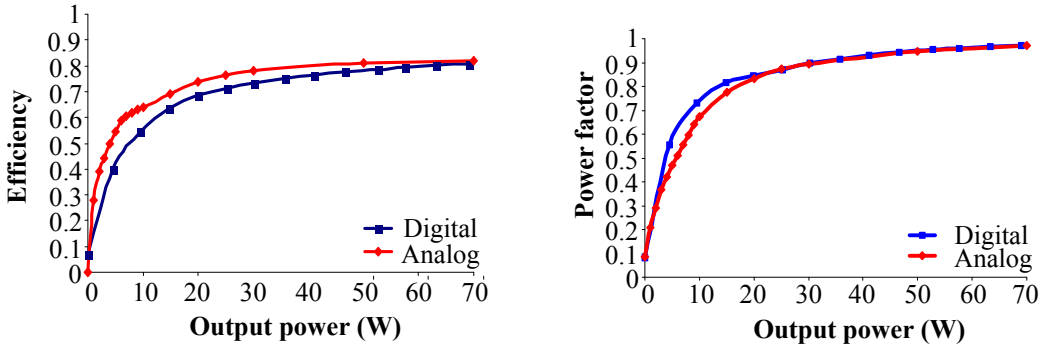


Figure 4.29: *Measure efficiency and power factor*

The two converters were also tested for conducted EMI. An Agilent N9010A EXA spectrum analyzer with a LISN network were connected to the AC line input of the converters (Figure 4.30)

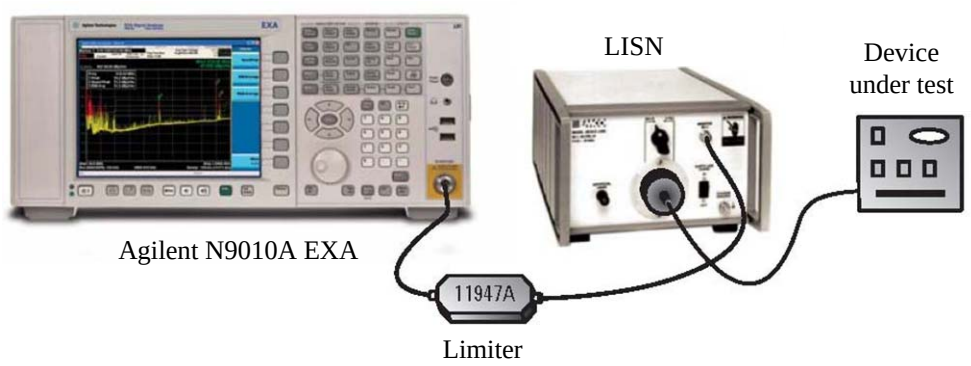


Figure 4.30: *Conducted emission measurement setup [109]*

As the test results show (Figure 4.31) both the analog and the digitally controlled converter emissions are under the limitations (IEC 55022 standard).

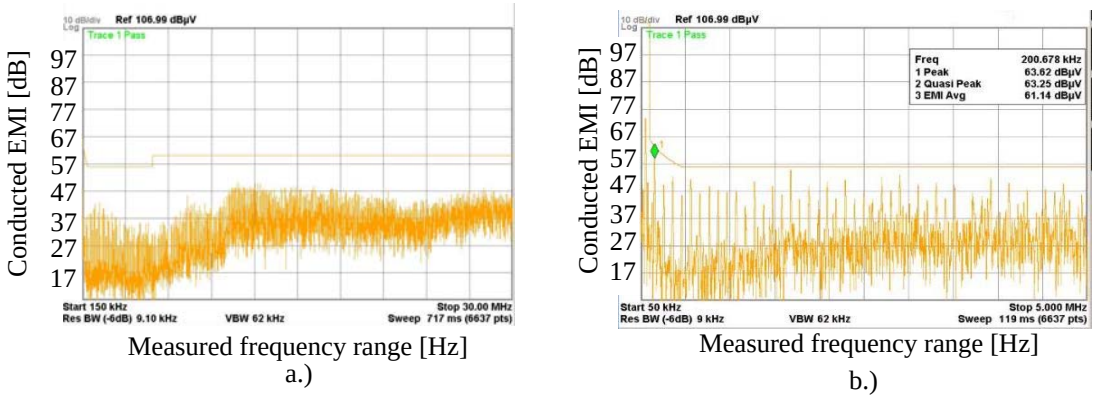


Figure 4.31: *Conducted EMI test results for a.) analog and b.) digital controlled converter*

The above comparison results were published and presented in "Efficiency and hardware comparison of analog control-based and digital control-based 70 W two-stage power factor corrector and DC-DC converters" - EPE 2011 - The 14th European Conference on Power Electronics and Applications - 2011, Birmingham, United Kingdom

As measurement results show the digital controller can compete with the analog one in performance. Analog controllers are cheap and robust and optimized for a specific application. If there are requirement changes, new controller has to be purchased which introduces additional cost issues. The major advantage of the digital controllers is that using the same controller with software modification new control strategies can be implemented if needed. One microprocessor is able to control a two-staged power factor corrector and DC-DC converter. Disadvantages are the cost issues (additional power supply) and lower efficiency at light load conditions in low power applications. Digital solution

might be an advantage at higher power levels because the few W additional supply loss might be insignificant in case of few hundred or thousand W power supplies.

4.2 600W Two-stage PFC/DC-DC power supply

A second step in implementing digital control for power factor corrector and DC-DC converters was designing, simulating and building a stand-alone, totally independent 600W two-stage converter with embedded digital controller for an LED based intelligent light source. The lamp consists of 12 (4 Red, 4 Green and 4 Blue) Luminus CBT-90 light emitting diodes (LEDs), connected in three strings (R, G and B). The three strings are controlled with three LED drivers (synchronous interleaved buck converters), supplying the required current (maximum 13.5A). The three strings are paralleled and connected to the second stage of the PFC/DC-DC converter through an LED driver.

A brief description of the lamp and its operation will be presented and published in "High Output LED-Based Profile Lighting Fixture" - IECON 2011 - 37th Annual Conference of the IEEE Industrial Electronics Society - 2011, Melbourne, Australia

4.2.1 Converter description

The system consists of an active rectifier and an isolated DC-DC converter connected in series. The topologies were chosen according to the output power requirements. For medium power application the two-stage power supply consists of a power factor corrector interleaved boost converter and an isolated phase-shifted full-bridge converter with current doubler.

Interleaved topology (Figure 4.32) was chosen for power factor correction to reduce the current stress on the boost inductors and switching devices as the coverter should operate at high line current.

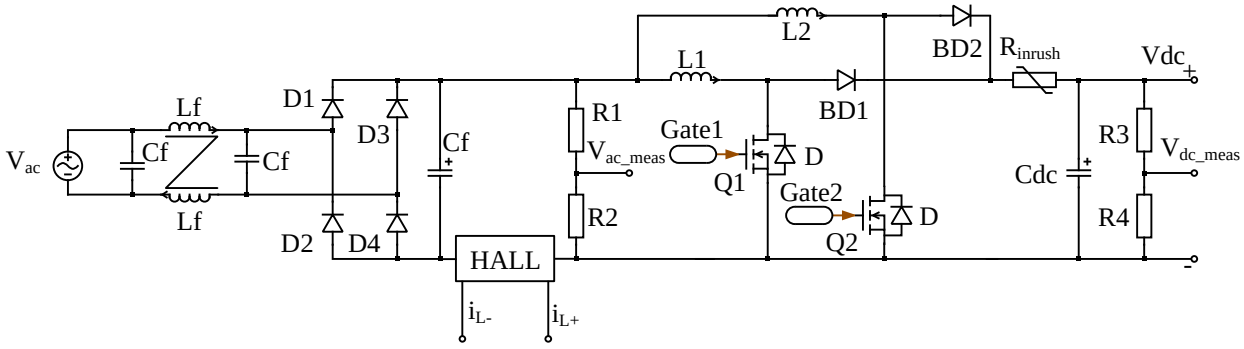


Figure 4.32: *Interleaved boost converter*

At medium and high power level phase-shifted full-bridge converter is a commonly used solution in DC-DC converter applications. As low voltage and high current are required to drive the LEDs, current doubler was chosen with synchronous rectification (Figure 4.33). This resulted in doubling the filter inductors but it was compensated with reduced current stress on each inductor, reducing the size of the magnetic cores. Also the transformer was rated to half of the output current thus smaller core could be used.

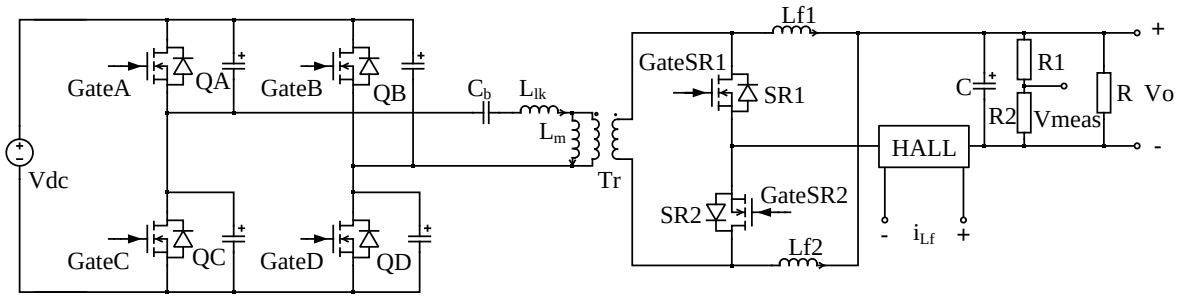


Figure 4.33: *Phase-shifted full-bridge converter with current doubler*

To meet the output requirements and overcome the effect of different losses the total input power of the two-stage converter is estimated to be around 700W so the boost inductors are with 10% overrated. As the two boost inductors are the two key components of the converter, different design parameters have to be taken into consideration. Firstly the peak inductor currents are the half of the peak line current. This determines the current ripples and the inductance values. Two Kool Mu material toroid cores from Magnetics were selected for boost inductors. These cores are recommended for high frequency operation.

Interleaved boost PFC converter design parameters	
V_{ac}	85-265 V
Vdc	400 V
Po	650 W
η	92%
f_L	40-60 Hz
f_s	100 kHz
$I_{peak\_L1} = I_{peak\_L2}$	$\frac{I_{peak\_tot}}{2}$
$\Delta I_{L1} = \Delta I_{L2}$	$25\% \cdot I_{L1}$

The above design parameters lead to the inductor value of L=700 μH, calculated with [81]:

$$L1 = \frac{(Vdc - V_{ac-min}) \cdot \frac{V_{ac-min}}{Vdc}}{2 \cdot \Delta I_1 \cdot f_s} \tag{4.25}$$

where Vdc is the output voltage, V_{ac-min} is the minimum input voltage, $\Delta I_{L1}, \Delta I_{L2}$, are the inductor current ripple and f_s is the switching frequency. As the output voltage Vdc is 400 V the boost transistor and diode were rated to 600V. To reach a compromise between the reduced output voltage ripple, the capacitor size and dynamic behavior of the system, two capacitors of Cdc=120 μF were paralleled as capacitive energy storage. A 5 Ω thermistor limits the inrush charging current of the capacitor at startup (Figure 4.32) (Design and core parameters presented in A.3)

The PSFB converter was designed to deliver in total 600W power with 35V output voltage. This means that the output current should be between 17-18A. To reduce the high current stress on the components a current doubler solutions was implemented. Though it doubles the number of the filter inductors their size and the current ripple in them can

be reduced. To reduce the voltage drop of the rectifier on the secondary side, synchronous rectification method was chosen.

Design parameters for the second-stage phase-shifted full-bridge converter:

Phase-shifted full-bridge converter design parameters	
V_{dc}	400 V
Po	600 W
Vo	35 V
η	95 %
f_s	100 kHz
$\Delta I_{Lf1} = \Delta I_{Lf2}$	$25\% \cdot \frac{Po}{Vo \cdot 2}$
D_{eff}	35%

The transformer turns ration is defined by the required output voltage, input voltage and the required operation duty cycle determined by the phase shift. Thus:

$$n = \frac{Vo}{Vdc \cdot D_{eff}} = 0.291 \tag{4.26}$$

where D_{eff} is the effective duty cycle, determined in Section 3.2.3. The transformer has a leakage inductance of $35\mu H$ (design in A.4). The full bridge transistors were rated to 600V, 3A while the synchronous rectifier MOSFETs to 200V and 20A.

With the desired current ripple, the output filter inductor value can be determined (the desired is $\Delta I_{Lf1} = 2.5A$) [81]:

$$Lf1 = Lf2 \geq \frac{(Vo + V_{switch}) \cdot (1 - D_{max})}{2 \cdot \Delta I_{Lf1} \cdot f_s} \tag{4.27}$$

where V_{switch} is the voltage drop on the synchronous rectifiers, D_{max} is maximum shift allowed (45% of the switching period). Thus the filter inductors have to be bigger than $40\mu H$. The inductor values were set to $Lf1 = Lf2 = 50\mu H$ and the two filter inductors were designed and built in laboratory on a Kool Mu material toroid cores. The two output capacitors having a total 4.4 mF filter the inductor current ripple and give smooth output voltage.

4.2.2 Controller design and description

The most suitable control strategy for both converters is the average current mode control. By using the sampled average values of the controlled currents and the output voltages the two control loops can be designed and implemented. The two converters have similar control structures: an internal current loop which gets the current reference from a lower bandwidth external voltage loop. To design the controllers, the small signal models had to be determined in Section 3.2.2 and 3.2.3.

4.2.2.1 Interleaved boost converter current loop design

Firstly the internal current loop design is presented. The sum of the two inductor currents is measured with a ACS712ELCTR-20A-T Hall-effect based linear current sensor and

scaled with operational amplifier to 0-3.3V. This gives a gain of $G_{HALL} = 0.577V/V$ This is included to the models' gain.

$$G_{id0} = \frac{2 \cdot Vdc}{D^2 \cdot R} \cdot G_{HALL} \tag{4.28}$$
$$D = 1 - \frac{V_{ac-min}}{Vdc}$$
$$D' = 1 - D;$$

where R represents the load resistance and D is the duty cycle according to the rectified line voltage. The duty cycle-to-inductor current transfer function is a second order system with one zero, similarly to the simple boost converter. It differs from the simple boost model with the component $L = L_p$, the paralleled value of the two inductors.

$$L_p = \frac{L1 \cdot L2}{L1 + L2} = 350\mu H \tag{4.29}$$

$$G_{id}(s) = G_{id0} \cdot \frac{\omega_n^2 \cdot (\frac{1}{\omega_{iz}} \cdot s + 1)}{s^2 + 2 \cdot \zeta \cdot \omega_n \cdot s + \omega_n^2} \text{ ,where} \tag{4.30}$$
$$\omega_n = \sqrt{\frac{D^2}{L_p \cdot C}} = 2.290 \cdot 10^3 \text{ rad/s} \tag{4.31}$$
$$2 \cdot \zeta \cdot \omega_n = \frac{1}{R \cdot C} = 10.68 \tag{4.32}$$
$$\omega_{iz} = \frac{2}{C \cdot R} = 21.36 \text{ rad/s} \tag{4.33}$$
$$G_{id0} = 2.587 \tag{4.34}$$

The ω_n is the undamped natural frequency and ζ is the damping ratio. Thus the plant's duty cycle-to-inductor current transfer function looks like:

$$G_{id}(s) = 2.587 \cdot \frac{5.247 \cdot 10^6 \cdot (0.0468 \cdot s + 1)}{s^2 + 10.68 \cdot s + 5.247 \cdot 10^6} \tag{4.35}$$

The converter is switched with 100kHz. Every second pulse generates a sampling sequence, thus the sampling frequency is 50kHz. In case of two phase interleaved boost converts the switching transistor of the second phase is operated with the same duty cycle as the first one, just it is turned on with a half period delay. The sampling sequence is generated by the first PWM generator and it appears always at the middle of the ON time of the first MOSFET. Thus an accurate sampling of the average current value can be performed and enough time is left for the ADC interrupt to update the controller output. According to this the discrete duty cycle-to-inductor current transfer function can be determined by using *Bilinear transformation* discretization method the continuous model

with $T_{si} = 20\mu s$. The obtained transfer function is:

$$G_{id}(z) = \frac{6.351 \cdot z^2 + 2.714 \cdot 10^{-3} \cdot z - 6.349}{z^2 - 1.998 \cdot z + 0.9998} \tag{4.36}$$

With the discrete transfer function the discrete controller can be designed. The goal is to obtain a controlled system with a closed loop bandwidth of close to 10 kHz.

Design requirements are similar, presented in Section 4.1.2.1:

- The maximum overshoot, which is equal to the maximum deviation of the step response of the system from the reference value should be smaller than 5%.
- At the open loop cutting frequency where the gain crosses the 0 dB, the phase margin should be higher than 60°.
- At the frequency ω_i where the phase of the open loop system crosses the $-180°$, the gain should be positive in dB.

The current control loop with PI controller is presented in Figure 4.8. Using the earlier defined design parameters, the discrete duty cycle-to-inductor current transfer function and discrete PI transfer function, the *Matlab SISOTOOL* toolbox was used to determine the Kpi and Kii values. The root-locus of open loop system was drawn and the controller parameters were adjusted such that the closed loop system has the required damping and crossover frequency with the desired phase margin. Thus:

$$Kpi = 0.11544$$
$$Kii = 0.04000$$

The root-locus and the open loop bode plot with the phase and gain margins of the controlled current loop is presented in Figure 4.34.

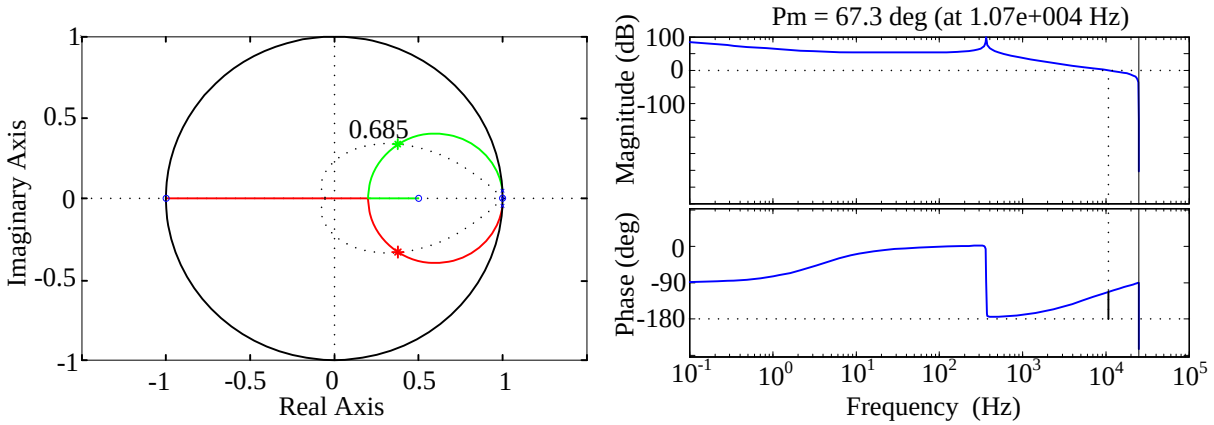


Figure 4.34: *Current loop - Root locus with closed loop poles and open loop bode diagram*

The closed loop poles are:

$$\begin{aligned} 0.9995; \\ 0.3748 + 0.3487j; \\ 0.3748 - 0.3487j; \end{aligned}$$

Thus the control loop's damping ratio is $\zeta = 0.666$ at the complex poles, allowing the system close to 5% overshoot and the phase margin $Pm = 67,3°$ at 10.7 kHz. All the resulted design parameters are within the requirement range so the chosen controller with the chosen control parameters it is able to deliver the required current loop dynamics.

4.2.2.2 Interleaved boost converter voltage loop design

The external low bandwidth control loop which gives the reference for the current loop is the voltage loop. Due to the rectified 50 Hz line voltage the output voltage will have a 100 Hz ripple. Thus the closed loop bandwidth was set to 10 Hz.

The duty cycle-to-output voltage transfer function (G_{vd}) was calculated in Section 3.2.2. The output voltage is measured through a voltage divider (V_{dc_meas}) and this is added to the gain of the transfer function:

$$\begin{aligned} G_{vd0} &= \frac{Vdc}{D'} \cdot R_{div} = 3.61 \\ R_{div} &= \frac{R_4}{R_3 + R_4} = 7.54 \cdot 10^{-3} \end{aligned} \tag{4.37}$$

The duty cycle-to-output voltage transfer function is similarly a second order system and it looks like:

$$G_{vd}(s) = G_{vd0} \cdot \frac{\omega_n^2 \cdot (-\frac{1}{\omega_{vz}} \cdot s + 1)}{s^2 + 2 \cdot \zeta \cdot \omega_n \cdot s + \omega_n^2} \text{ ,where} \tag{4.38}$$

$$\omega_n = \sqrt{\frac{D'^2}{L \cdot C}} = 2.290 \cdot 10^3 \text{ rad/s} \tag{4.39}$$

$$2 \cdot \zeta \cdot \omega_n = \frac{1}{R \cdot C} = 10.68 \tag{4.40}$$

$$\omega_{vz} = \frac{D'^2 \cdot R}{L} = 4.911 \cdot 10^5 \text{ rad/s} \tag{4.41}$$

$$\tag{4.42}$$

The sampling frequency of the output voltage is 5 times lower than the one of the current. Thus the discrete mode uses a $T_{sv} = 100\mu s$ as sampling time. The resulted discrete $G_{vd}(z)$ transfer function is:

$$G_{vd}(z) = \frac{0.04491 \cdot z^2 + 0.09364 \cdot z + 0.04873}{z^2 - 1.947 \cdot z + 0.9989} \tag{4.43}$$

The transfer function of the system can be derived from the duty cycle-to-output voltage, duty cycle-to-inductor current and the current PI controller as shown in Figure 4.11. The closed current loop combined with the duty cycle-to-output voltage transfer function:

$$G_{sysv}(z) = \frac{PIi(z)}{1 + PIi(z) \cdot G_{id}(z)} \cdot G_{vd}(z) \tag{4.44}$$

The resulting combined transfer function is:

$$G_{sysv}(z) = \frac{1.3 \cdot 10^{-3} \cdot z^3 + 3.05 \cdot 10^{-3} \cdot z^2 + 2.1 \cdot 10^{-3} \cdot z + 0.37 \cdot 10^{-3}}{z^3 - 0.02504 \cdot z^2 - 0.6354 \cdot z - 0.3346} \tag{4.45}$$

The voltage PI controller design requirements are similar to the current controller requirements. The only difference is the voltage overshoot, which should be smaller than 2.5%. The *Matlab SISOTOOL* toolbox was used to determine the Kpv and Kiv values. The root-locus of open loop system was drawn and the controller parameters were adjusted such that the closed loop system has the required damping and crossover frequency with the desired phase margin. Thus:

$$Kpv = 0.99998$$
$$Kiv = 0.00500$$

The root-locus and the open loop bode plot with the phase and gain margins of the controlled system is shown in Figure 4.35.

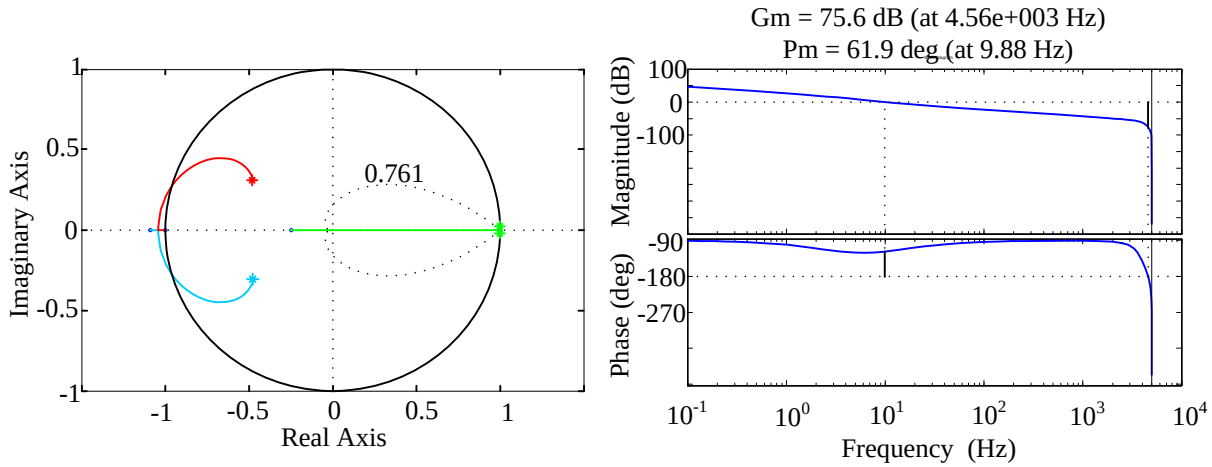


Figure 4.35: *Voltage loop - Root locus with closed loop poles and open loop bode diagram*

The closed loop poles of the voltage loop are:

$$0.9984 + 2.2779e - 3j;$$
$$0.9984 - 2.2779e - 3j;$$
$$-0.486 + 0.3143j;$$
$$-0.486 - 0.3143j;$$

The two dominant poles give the closed voltage control loop a damping factor of $\zeta = 0.81$ and a phase margin of $Pm = 83°$ at 9.38 Hz.

4.2.2.3 Phase-shifted full-bridge converter current loop design

The phase-shifted full-bridge converter is modeled as an interleaved synchronous buck converter. Detailed description of its operation and modeling can be found in Section 3.2.3. The input voltage for the model is the voltage on the secondary side of the transformer. To control the output current and voltage of the PSFB converter, the sum of the filter inductor currents and the output voltage is measured (Vmeas - Figure 4.33) and used as a feedback for the controller. The current is measured with a ACS756SCA-050B Hall-effect current sensor and scaled to 0-3.3V with operation amplifier resulting in a gain of $G_{HALL} = 0.11$ The total current loop gain is:

$$G_{id0} = \frac{n \cdot Vdc}{R} \cdot G_{HALL} = 5.5 \tag{4.46}$$

where Vdc=400V is the input voltage from the boost capacitor, R represents the load and n is the transformer turns ratio. Based on the earlier developed model, the duty cycle-to-inductor current transfer function at full load:

$$G_{id}(s) = G_{id0} \cdot \frac{C \cdot R \cdot s + 1}{L \cdot C \cdot s^2 + (Z_b \cdot C + \frac{Lp}{R}) \cdot s + \frac{Z_b}{R} + 1} \tag{4.47}$$

where $Z_b = 2 \cdot n \cdot L_{lk} \cdot F_s$. The leakage inductance is $36\mu H$ and Lp is the paralleled output filter inductor ($Lf1 = Lf2 = 51\mu H$). Thus Gid becomes:

$$G_{id}(s) = \frac{0.04248 \cdot s + 5.559}{1.133 \cdot 10^{-7} \cdot s^2 + 7.172 \cdot 10^{-3} \cdot s + 1.937} \tag{4.48}$$

The sampling frequency is 50 kHz ($T_{si} = 20\mu s$). Using the Bilinear transformation method and sampling the continuous transfer function with T_{si}, the discrete transfer function results as:

$$G_{id}(z) = \frac{2.297 \cdot z^2 + 0.006 \cdot z - 2.291}{z^2 + 1.221 \cdot z + 0.2255} \tag{4.49}$$

The fast current loop is controlled with PI controller. The Matlab SISOTOOL toolbox was used to determine the PI parameters. The root-locus of the open loop system was drawn and the controller parameters were adjusted such that the closed loop system has the required damping and crossover frequency with the desired phase margin. Thus:

$$Kpi = 0.08000$$
$$Kii = 0.00800$$

The root-locus and the open loop bode plot with the phase and gain margins of the controlled current loop is presented in Figure 4.36.

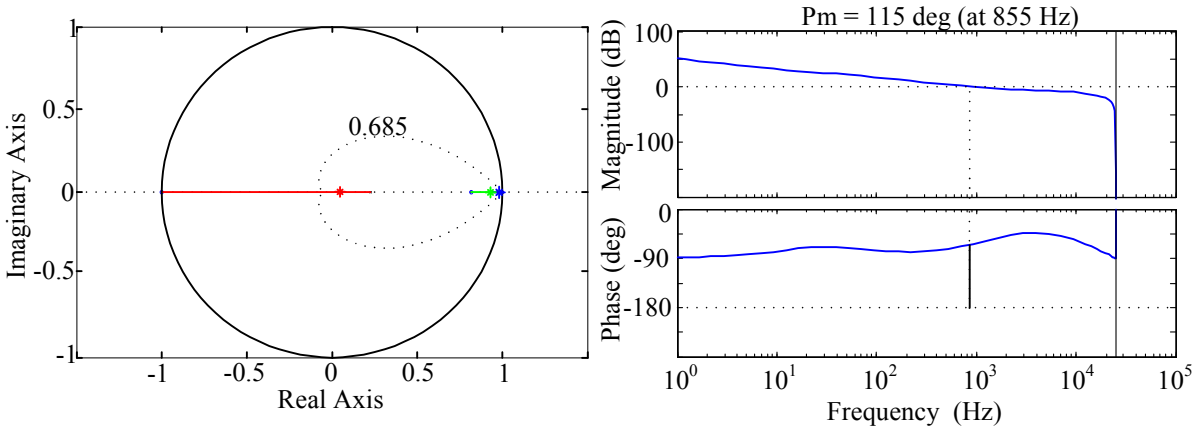


Figure 4.36: *Phase-shifted full-bridge converter - current loop design*

The closed loop poles are:

$$0.9974;$$
$$0.9333;$$
$$0.0540;$$

As all the poles are real numbers, the damping factor is $\zeta = 1$. The phase margin is $Pm = 115°$ at 855 Hz. The system is able to follow load changes with close to 1 kHz frequency.

4.2.2.4 Phase-shifted full-bridge converter voltage loop design with PI controller

To control the output voltage of the PSFB converter, different control solutions were tried. Firstly a PI controller was designed and tested. Firstly the small signal transfer function had to be determined. The natural gain of the duty cycle-to-output voltage is:

$$G_{vd0} = n \cdot Vdc \cdot R_{div} = 6.5$$
$$R_{div} = \frac{R2}{R1 + R2} = 7.4 \cdot 10^{-2}$$

$$G_{vd}(s) = G_{vd0} \cdot \frac{1}{L \cdot C \cdot s^2 + (Z_b \cdot C + \frac{Lp}{R}) \cdot s + \frac{Z_b}{R} + 1} \tag{4.50}$$

where Z_b is described in Section 4.2.2.3. Substituting the converter parameters in the transfer function, it becomes:

$$G_{vd}(s) = \frac{6.5}{1.133 \cdot 10^{-7} \cdot s^2 + 7.172 \cdot 10^{-3} \cdot s + 1.937} \tag{4.51}$$

The sampling time for the discrete voltage G_{vd} transfer function was $T_{sv} = 200\mu s$. Thus the discrete duty cycle-to-output voltage transfer function:

$$G_{vd}(z) = \frac{0.07651 \cdot z^2 + 0.153 \cdot z + 0.07651}{z^2 + 1.221 \cdot z + 0.6878} \tag{4.52}$$

The resulted transfer function has to be combined with the closed current loop transfer function:

$$G_{sysv}(z) = \frac{6.762 \cdot 10^{-3} \cdot z^3 + 13.52 \cdot 10^{-3} \cdot z^2 + 6.762 \cdot 10^{-3} \cdot z + 7.491 \cdot 10^{-16}}{z^3 - 0.6629 \cdot z^2 - 0.6939 \cdot z + 0.38} \tag{4.53}$$

The discrete PI controller was designed with Matlab SISOTOOL toolbox, by adjusting the PI parameters to meet the required design parameters on the root locus and the bode plot of the open voltage loop. Thus the Kpv and Kiv are:

$$Kpv = 0.99998$$
$$Kiv = 0.01000$$

The root-locus and the open loop bode plot with the phase and gain margins of the controlled system is shown in Figure 4.37.

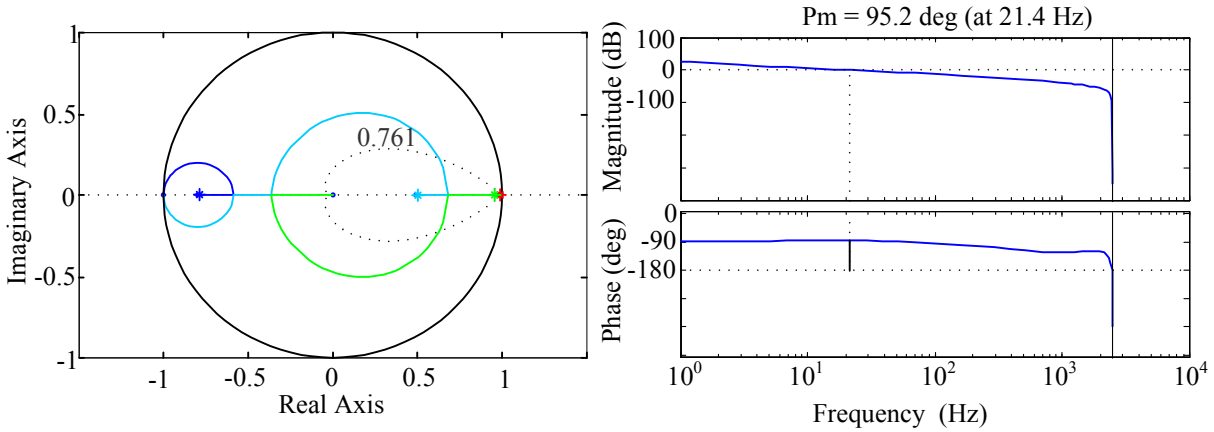


Figure 4.37: *Phase-shifted full-bridge converter - voltage loop design with PI controller*

The closed loop poles:

$$0.7993;$$
$$0.9853;$$
$$0.9594;$$
$$0.4993;$$

As all the poles are real numbers, the damping factor is $\zeta = 1$. The phase margin is $Pm = 95.2°$ at 21.4 Hz.

4.2.2.5 Phase-shifted full-bridge converter voltage loop design with Fuzzy controller

To reduce the number of analytical calculations for determining the Gvd transfer function, a simple fuzzy logic voltage controller is proposed. The control will work based on two input sets: the output voltage error ($ev(k) = V_{ref} - Vdc(k)$) and the error variations ($dev(k) = ev(k) - ev(k-1)$) which are sampled every $200\mu s$. The k is the actual sampling sequence. The basic control structure is shown in Figure 4.38.

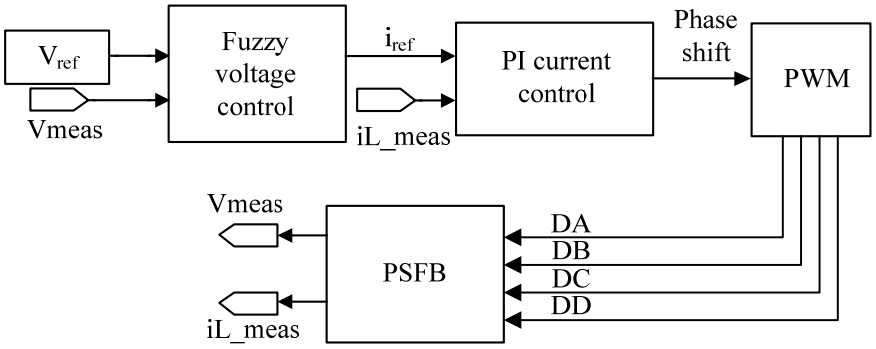


Figure 4.38: *Block diagram of the Fuzzy control system*

For both the voltage error and error variation five triangle membership functions were assigned with 50% overlap. These functions represent the rule base of the fuzzy system and correspond to the size of the error/error variation: NB-negative big, NS-negative small, Z-zero, PS-positive small and PB-positive big. The size of ev and dev are compared to the reference voltage (V_{ref}). The error is considered maximum at startup, when it is V_{ref}. This corresponds to PB, the actual voltage level is lower than the reference. A maximum overshoot of reference voltage size is allowed in the worst case. In this case the error is $-Vref$, thus the output voltage is over the reference (NB). Two intermediate error levels are also included, $NS = -V_{ref}/4$ and $PS = V_{ref}/4$. When the voltage error is zero than, this state belongs to the $Z = 0$ membership function (Figure 4.39). For the error variation the $NB = -V_{ref}/8$, $NS = -V_{ref}/16$, $Z = 0$, $PS = V_{ref}/16$ and $PB = V_{ref}/8$ (Figure 4.40). These values allow much less error variation compared to the reference voltage, thus the sensitivity of the voltage controller to voltage variation is much bigger.

To decide which membership function one measured value belongs to and in what weight, simple percentage calculations are used. Firstly it is determined the interval where the error and the error variation is in. It is determined in percentage, how far it is the point from one end of the interval. This is the weight the error and the error variation belongs to a membership function belongs with. The calculations start from the point 0 to the left and to the right. Each membership function has the peak value, 1, at the five error and error variation points defined earlier. At the maximum points the belonging weight is 100% to the respective membership function and 0% to all its neighbors. Between two peaks the error and error variations belong to two neighbor membership functions in different percentage.

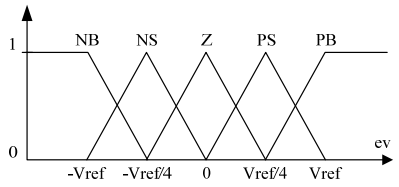


Figure 4.39: *The voltage error ev membership functions*

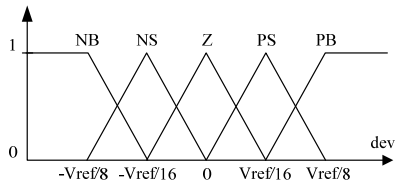


Figure 4.40: *The voltage error dev membership functions*

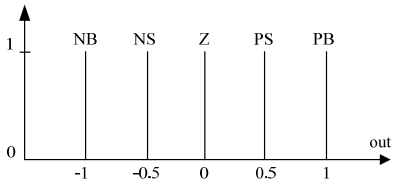


Figure 4.41: *Output singleton membership functions*

Based on Sugeno fuzzy system, the output membership functions are singletons (Figure 4.41) ([113] pp. 156). Their meaning is $NB - negativebig$ - control signal has to be decreased significantly up to $PB - positivebig$ where control signal has to be increased significantly. The output vector is chosen out = [-1,-0.5,0,0.5,1] with indexing from NB to PB. A table called *Inference table - I* contains the possible combinations which define the output control action. Based on the error and error variation this looks like:

	ev(k)					
dev(k)		**NB**	**NS**	**Z**	**PS**	**PB**
	NB	PB	PB	PS	PS	Z
	NS	PB	PS	PS	Z	NS
	Z	PS	PS	Z	NS	NS
	PS	PS	Z	NS	NS	NB
	PB	Z	NS	NS	NB	NB

Table 4.2: *Inference table - I*

Evaluating the inference table the output is the min(dev(k), ev(k)). As an example:

If $dev(k) = NS$ and $ev(k) = PS$ then $\mu(NS, PS) = min(dev(k), ev(k))$

In the above example μ is the weighting table for the output, it has the same size and indexing as the inference table and this will be used in defuzzification. The final output value is obtained by using the weighted average method: multiplying the weighting table elements with the corresponding output values.

$$du(k) = \frac{\sum_{i=NB,j=NB}^{PB} \mu(i,j) \cdot out(I(i,j))}{\sum_{i=NB,j=NB}^{PB} \mu(i,j)} \tag{4.54}$$

where I is the inference table. With the obtained $du(k)$ the control signal for the next control sequence can be obtained as:

$$u(k) = du(k) + u(k-1) \tag{4.55}$$

In practice only maximum four fields of the weight table will be nonzero. This is due to the fact that in one control sequence the error and the error variation can belong only to two membership functions at the same time. Thus the calculations can be reduced by monitoring which of these four fields is *active*, nonzero. This is used to reduce the calculation time in the digital controller implementation. The fuzzy incremental controller (Figure 4.42) is almost like a PI controller [111].

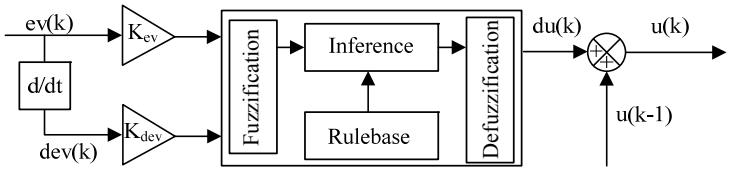


Figure 4.42: *Fuzzy incremental control block*

The output of the controller can be defined as:

$$\begin{aligned} u(k) &= \sum_{i=1}^{k} (K_{ev} \cdot ev(i) + K_{dev} \cdot dev(i)) \cdot T_{sv} \\ &= \sum_{i=1}^{k} (K_{ev} \cdot ev(i) + K_{dev} \cdot \frac{ev(i) - ev(i-1)}{T_{sv}}) \cdot T_{sv} \\ &= K_{ev} \sum_{i=1}^{k} \cdot ev(i) \cdot T_{sv} + K_{dev} \cdot ev(k) \end{aligned} \tag{4.56}$$

The above equation is very similar to the discrete PI equation, thus the fuzzy incremental control parameters can be assigned as:

$$\begin{aligned} K_{ev} &= K_{iv} \\ K_{dev} &= K_{pv} \end{aligned}$$

where K_{iv} and K_{pv} are the voltage PI controller parameters, designed in Section 4.2.2.4.

A comparison of the converter behavior using PI and Fuzzy voltage controller is presented and published in "Digital Fuzzy logic and PI control of phase-shifted full-bridge current-doubler converter" The International Telecommunications Energy Conference 2011, Amsterdam, The Netherlands.

4.2.3 Simulations

Large signal model of the converters were built in Matlab/Simulink with the embedded PLECS toolbox to simulate the converter behavior with the designed control algorithms.

4.2.3.1 Interleaved boost converter

The interleaved boost converter PLECS model is presented in Figure 4.32. The model considers the on-resistances of the rectifier, switching MOSFETs and diodes. The series resistance of the boost inductors is modeled as well as the line impedance. Electromagnetic interference (EMI) filter is also taken into consideration at simulations. A common mode choke and its leakage inductance with two X capacitors are included. The line voltage is sinusoidal, 50 Hz, and includes the additional harmonic components measured in the university laboratory (Table 4.1).

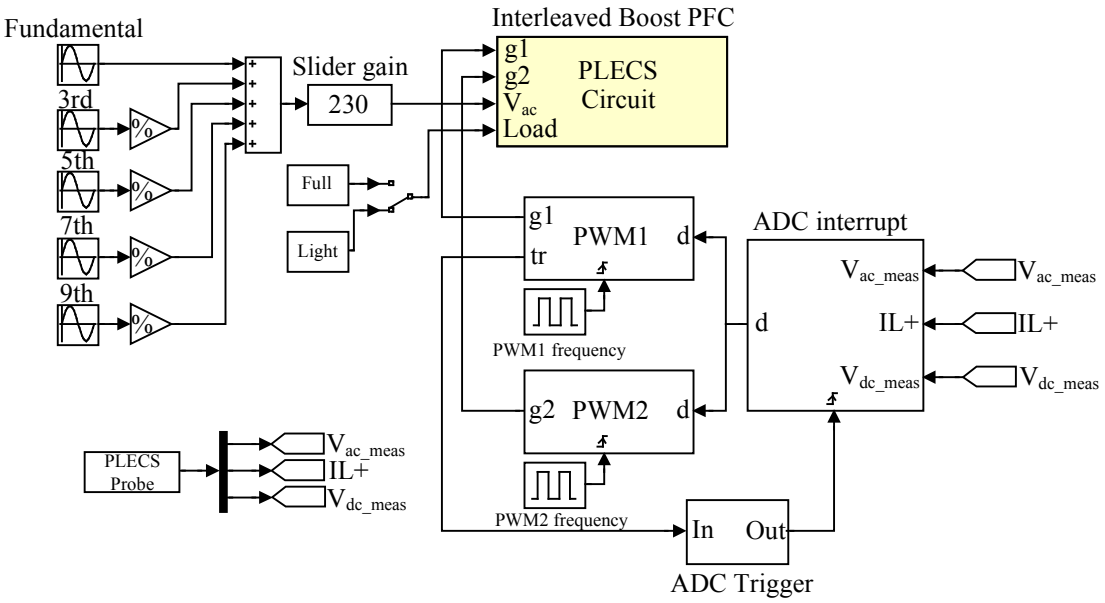


Figure 4.43: *Simulation blocks for interleaved boost converter*

The measured values ($V_{ac\_meas}, V_{dc\_meas}, i_{L+}$) are scaled according to the real converter design and the microprocessor Q.15 requirements. In simulation the HALL sensor is modeled with a series resistor with the real amplification value. To verify the converter behavior to universal line voltage, in PLECS a controlled voltage source serves as input voltage source, controlled from Simulink (Figure 4.43). The input sinusoidal waveform is a sum of the fundamental (50 Hz) and odd harmonics (3^{th}, 5^{th}, 7^{th}, 9^{th} and 11^{th} were present

in significant percentage in the measured line voltage) sinusoidal waveforms. The input voltage RMS value is determined by sliding bar gain from 85 to 265 V. To generate different load steps a manual switch was added to the model, switching between different load resistors.

The three measured values are sampled and processed in the *ADC interrupt* block. The interrupt is triggered every second switching sequence by the first gate signal ($PWM1$) in the middle of the ON-time of the MOSFET. The *ADC trigger* block solves the frequency reduction. The second gate signal ($PWM2$) is shifted with half switching period and uses the same duty cycle value. The PWM generators and the ADC interrupt block are embedded Matlab functions. In the PWM generator it is compared the d duty cycle value to a ramp. This counter reaches its maximum value, determined by the PWM frequency block, and than is reset exactly in $10\mu s$.

The ADC interrupt is divided in two sections. First section is the current control loop, which processes the sampled $IL+$ and V_{ac_meas} in every trigger sequence and calculates the duty cycle. The other one, which is activated every 5^{th} trigger sequence, is the DC link voltage sampling. This part calculates the voltage controller parameters. This output of the voltage controller is multiplied with the V_{ac_meas} according to the Q.15 rules, thus generating the sinusoidal current reference with the right amplitude.

All data is stored and processed according to the rules of the Q.15 arithmetic as the algorithm has to be implemented on a 16 bit fixed point dsPIC microprocessor. That explains why the PI controller coefficients are numbers between 0 and 1. Sometimes this might be also a limitation to the dynamics of the system, as the current setup cannot handle higher controller gains then $Kp = 0.99998$ which corresponds to 32767 as the 16 bit signed integer maximum.

Simulation results are presented in Figures 4.44-4.45. Figure 4.44 a.) shows the normalized line voltage with the normalized sinusoidal line current. The line voltage is $230V_{RMS}$ while the line current $2.99A_{RMS}$. Figure 4.44 b.) show the two boost inductor currents and the sum of them (red).

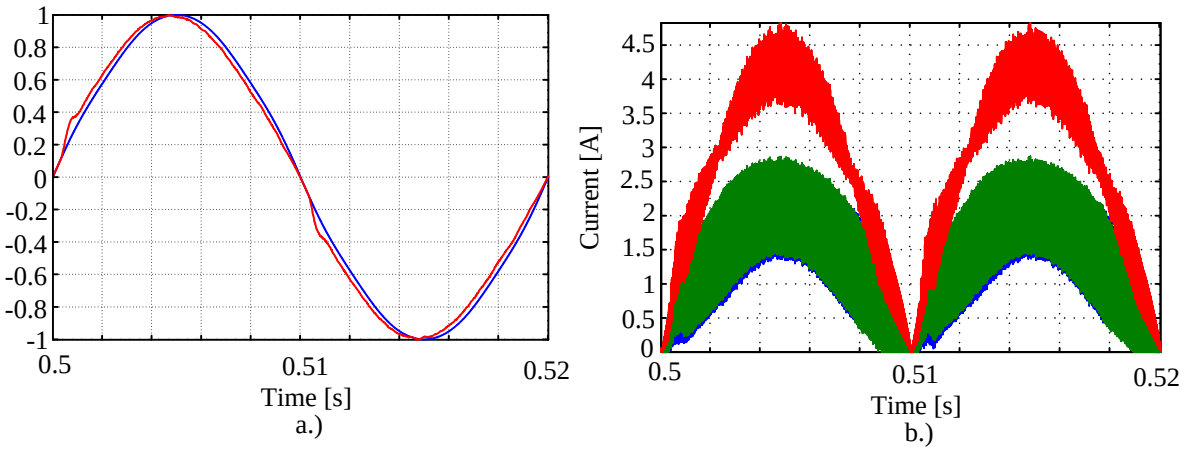


Figure 4.44: *a.) Normalized line voltage (blue) and line current (red) b.)Boost inductor currents (blue and green) and the total inductor current (red)*

Figure 4.45 presents the harmonic content of the line current. A total harmonic dis-

tortion of 3.1% is present. Thus the distortion factor is $K_d = 0.9995$. Also a displacement between the line current and the voltage is visible, resulting in a displacement factor of $cos\phi = 0.9764$. The total power factor is:

$$PF = K_d \cdot \cos\phi = 0.97644 \tag{4.57}$$

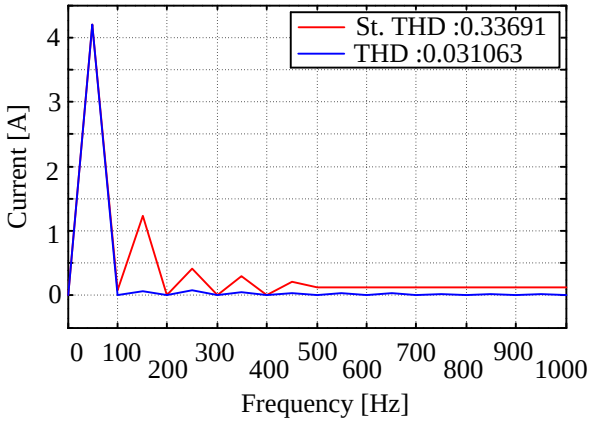


Figure 4.45: *Line current harmonics compared to EN 61000-3-2 Class C.*

4.2.3.2 Phase-shifted full-bridge converter with current doubler and synchronous rectification

The PLECS model of phase-shifted full-bridge converter with current doubler is presented in Figure 4.33. The model considers the on-resistance and the parasitic capacitance of the switching transistors and the series resistance of the leakage inductor, transformer magnetizing inductance and output filter inductors. A snubber is included in parallel with the secondary winding of the transformer to damp the ringing caused by the leakage inductance and the parasitic capacitances.

The sum of the inductor currents and the output voltage is measure on the secondary side and used as feedback for the control algorithm. The HALL sensor is modeled with an equivalent resistor with the value of the $G_{HALL} = 0.11$. The output voltage is measured with a voltage divider, resulting in a gain of $R_{div} = 0.074$. With these gains the measured values are scaled between 0-3.3 V.

The input voltage is 395 V, the voltage of the boost capacitor. It has a 100 Hz ripple with an amplitude of 5 V. To test the behavior of the converter with different loads and the dynamics for different load changes, three different resistors were connected to the output and with a switch it can be selected manually the required load.

Simulation block diagram of the DC-DC converter and control system is presented in Figure 4.47. The PLECS circuit has 8 inputs: the four gate signals for the full bridge (GA-GD), two gate signals for the synchronous rectifier. The GSR1=GC and GSR2=GA [114] as it is simple to implement in the microprocessor. The PWM signals also include dead time. For the leg1 a total of 360 ns (180 ns at turn-on and 180 ns at turn-off) is added. For leg2 160 ns dead time is considered for each transistor (80 ns for turn-on and 80 ns for turn-off). The last two inputs are the required 395 V DC voltage with 100Hz

ripple and the load steps. The measured filter inductor current (iL_meas) and the output voltage ($Vmeas$) are sampled by the ADC interrupt and Fuzzy functions.

The *ADC interrupt* and *Fuzzy* function block are triggered by every second GA pulse (*ADC trigger* block is described in Figure 4.16). The current is sampled with $T_{si} = 20\mu s$ and the voltage by $T_{sv} = 200\mu s$. The current is controlled by PI controller, implemented in the *ADC interrupt* in form of an embedded Matlab function in a triggered subsystem. The output of the current loop is a value which represents the phase shift between the switching patterns of the leg A-C and leg B-D. This value is processed in a the *PWM generator* block. Two counters are determining the PWM pulses for the two legs and the duty cycle value for the secondary voltage. When the second counter, which is responsible for leg B-D, reaches the Shift value it is reset. After it both counters, having different values, are compared to the duty cycle value (0.5) and pulses are generated. This is very similar to the PWM counters and shifting in the microcontroller thus the internal behavior of the dsPIC is simulated. The PWM resolution determined by the *PWM frequency* pulse generator is limited to reduce the simulation's calculation time.

Firstly the converter behavior was tested as shown in Figure 4.46. Fixed duty cycle and fixed phase-shift was used to check the converter waveforms. The model was developed parallel with starting up the controller and power board. Thus the effect of the dead time is visible also in simulation on the voltage in the primary winding of the transformer. The effect of the leakage inductance and MOSFET internal capacitances are visible in form of ringings on the transformer currents and secondary side drain-source voltages. This ringing can be damped by an RC snubber, parallel with the secondary winding. Simulation model includes serial resistances for the inductors, ON resistances and internal capacitances for the switching devices.

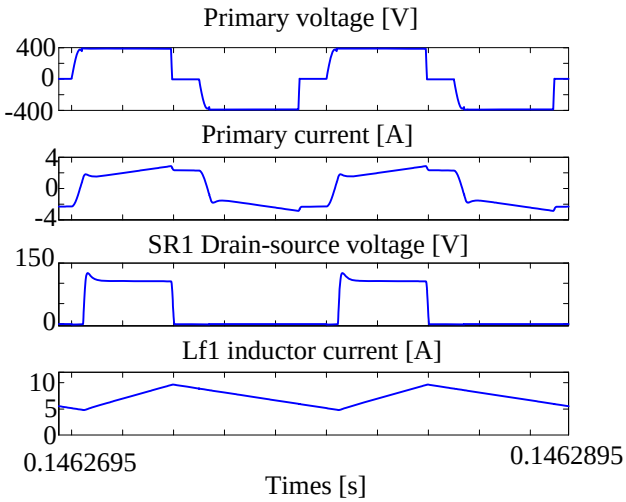


Figure 4.46: *600W PSFB simulated waveforms*

Two control algorithms were designed and tested to control the output voltage and determine the reference current for the current loop. One PI controller which was implemented in the *ADC interrupt* block and one Fuzzy algorithm, described in 4.2.2.5. It can be selected manually which voltage control algorithm should determine the reference

current. Thus identical conditions were created in order to compare the performance of the two control algorithms.

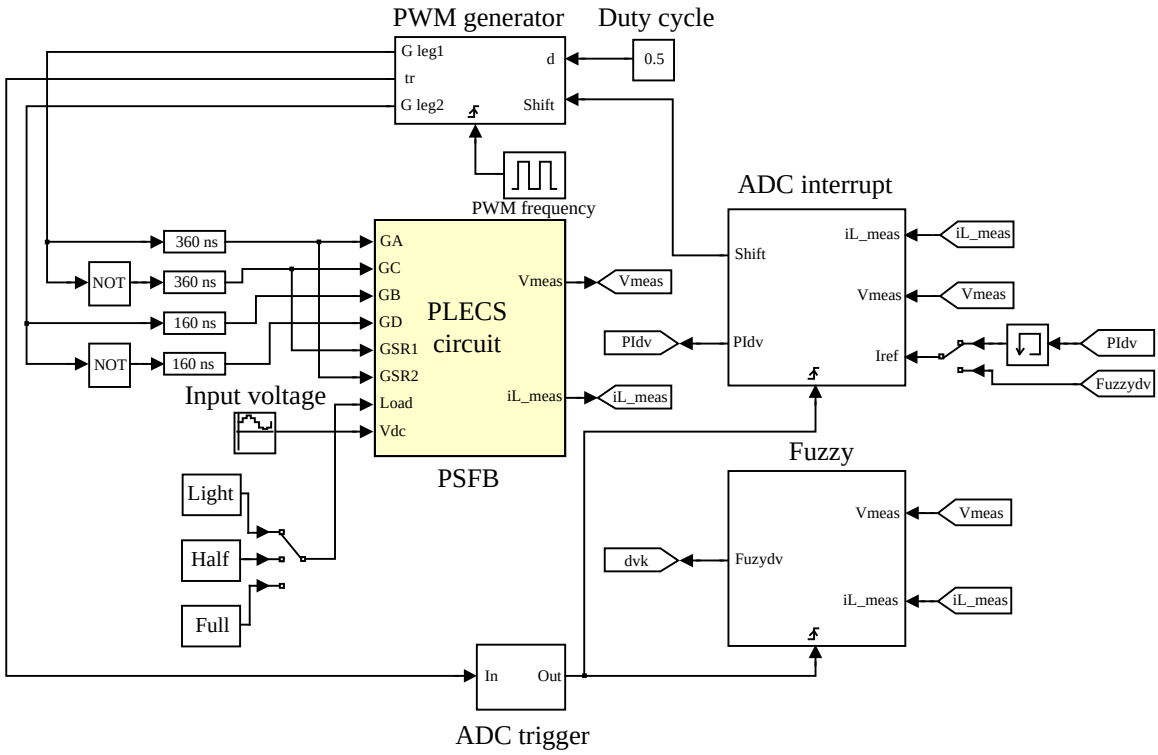


Figure 4.47: *Phase-shifted full-bridge converter - simulation blocks*

In Figure 4.48 some load-steps using fuzzy controller from full load to half load, then down to no load and back to full load (600W) are shown. The same conditions are presented in Figure 4.49. In this case the output voltage is controlled by PI controller. The same parameters were used for the fuzzy and PI controllers, described in Section 4.2.2.4. and Section 4.2.2.5. The difference in dynamics is visible. In case of fuzzy control the output voltage has smaller overshoots at power variations and its settling time is 40 ms. The inductor current shows higher overshoot. For the same conditions the PI control has the same settling time but there is higher voltage overshoot due to slower current rise.

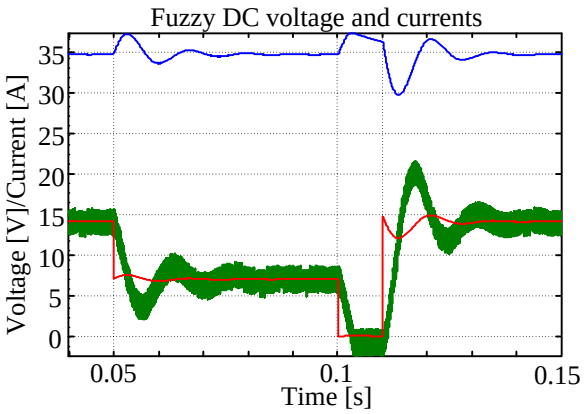


Figure 4.48: *Load step with Fuzzy controlled voltage loop: blue - output voltage (V), green - summed filter inductor current (A), red - output current (A)*

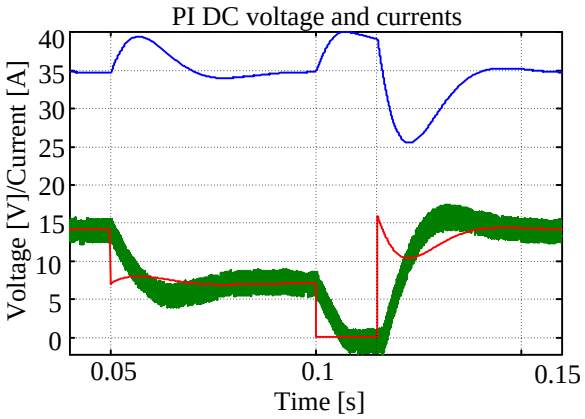


Figure 4.49: *Load step with PI controlled voltage loop: blue - output voltage (V), green - summed filter inductor current (A), red - output current (A)*

The presented design and the chosen 16 bit fixed point microcontroller put some limitations to the controller performance. The gain of the voltage PI controller reached its maximum value in Q.15 format. With this conditions were the two control strategies compared.

Though the PI controller is faster considering the calculation time, the fuzzy controller with the same parameters shows better response to load changes (smaller load voltage and current overshoot). Other advantage of using fuzzy controller is that less analytical calculations are required as the decisions made with this control strategy are based on empirical knowledge. Disadvantage is the computational time, compared to PI's at such high sampling and switching frequency. This reduces its applicability to low bandwidth control loops.

4.2.4 Digital control implementation

One of the main goals in the converter design was to use a single digital control with multiple PWM outputs to control at the same time the primary interleaved boost PFC and

the secondary PSFB DC-DC converter with current doubler and synchronous rectification. For this purpose a Microchip dsPIC33FJ32GS406 was embedded to the power PCB (Figure 4.50) [115]. The 3.3V supply voltage (VDDx) is generated by a small auxiliary power supply. The ground (VSSx) is the ground of the primary side.

The programming of the dsPIC is done with a Microchip ICD2 In-circuit debugger, connected to the PCB through an RJ11 6 pin socket [116]. Beside the VCC, VDD and $\underline{MCLR}$ the clock pulses and serial data is are sent from the ICD2 to the dsPIC through pins PGEC1 (clock) and PGED1 (data) pins. A reset pushbutton is connected to the $\underline{MCLR}$ pin in order to allow hard reset of the controller. A Status LED always shows that the supply voltage is present and the controller settings are done properly.

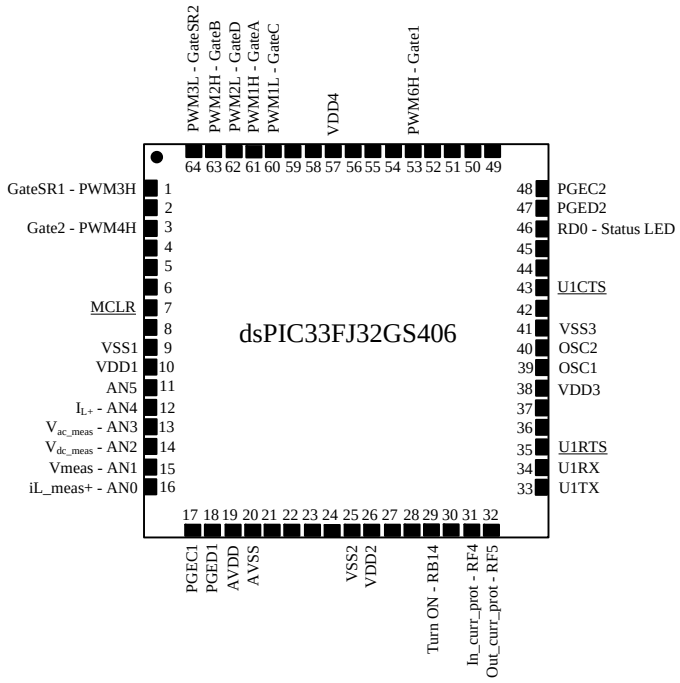


Figure 4.50: *dsPIC33FJ32GS406 microcontroller*

The microcontroller is placed on the primary side thus it is isolated from the load. Two PWM signals (PWM4H and PWM6H) are driving the interleaved boost MOSFETS. PWM1H/L and PWM2H/L give the pulses to the full bridge MOSFETS. The shift between PWM1 and PWM2 is determined by the control algorithm. The synchronous rectifiers are synchronized to PWM1 just PWM3H=PWM1L and PWM3L=PWM1H. To control the PFC converter the sum of the inductor current (I_{L+}), rectified line voltage (V_{ac_meas}) and the DC link capacitor voltage (V_{dc_meas}) is measured. These values are processed with the fast 10 bit analog-to-digital converter of the dsPIC. The firmware was developed in Microchip Mplab code composer in C language based on the Matlab simulation code. The boost converter control algorithm (current loop and voltage loop) was placed in an ADC interrupt, triggered in the middle of every second pulse of PWM4H.

The control variables for the phase-shifted full-bridge converter are iL_meas+ - the sum of the filter inductor currents and $Vmeas$, the output voltage on the load side. Both sampled by the 10 bit ADC converter. To obtain an exact value of the output voltage

and process it on the primary side linear analog optocouplers should be used. On the idea of the linear analog optocouplers [110], which cost from 20 (mass purchase unity price) up to 38 (unity price) DKK (Farnell database), two low-cost 4N36 (price from 1.69 to 5 DKK) optocouplers were used with the same driving current (Figure 4.51).

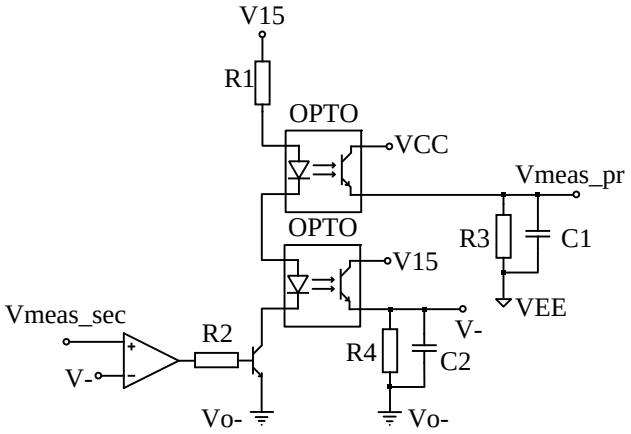


Figure 4.51: *Controlled optocoupler for voltage measurement*

One will deliver the output to the microcontroller on the primary side ($Vmeas\_pr$), identical to the measured output voltage on the secondary side. The second one is used as a feedback signal ($V-$) and being compared to the measured output voltage ($Vmeas\_sec$). The comparator will drive a transistor allowing the required current magnitude to flow through the optocouplers. Thus an exact value of the measured load voltage can be sampled on the primary side. The two optocouplers were placed close to each-other to have similar environmental conditions.

The current control loop is placed in an ADC interrupt. This is synchronized and triggered by every second PWM1H pulse. The current PI controller parameters are updated every interrupt, allowing the output inductor current a fast response to load changes. To control the output voltage two control algorithms were developed and tested. The classical PI controller was used in the first case, along with the current loop in the same interrupt. The voltage was sampled and the voltage PI parameters were updated every 10^{th} interrupt. As a second solution, a digital fuzzy logic controller was proposed and implemented to control the output voltage. As the fuzzy algorithm has to make lots of decisions and calculate the output values based on the inference table the fuzzy code was placed in the main loop, allowing time for the interleaved boost control and PSFB current control ADC interrupts.

The algorithm starts with the initializing sequences. The oscillator, the 8 PWM outputs and the 5 analog input channels are initialized and if everything is checked the Status LED ($RD0$) turns on green and with $RB14 = 1$ a relay turns the power on the main line.

Before starting the control algorithms it had to be checked that all the measured data corresponds to the expectations and are within the limits. For this purpose a small Matlab script was developed. This is working as a digital oscilloscope. It reads back with an ICL3232CWZ RS-232 IC from the UART modul of the dsPIC the sampled values and plots them on the computer screen. This feature can be used in later developments to

make loggings in the power supplies and evaluate their operation by connecting them to a centralized server.

4.2.5 Auxiliary power supply

Using a digital signal processor, an external gate driver is needed. Also dsPIC33Fx microcontrollers have a very narrow voltage tolerance ($VDD = 3 - 3.3$ V), thus it requires a stable supply voltage. An additional small flyback converter controlled with a LinkSwitch LNK562 switch was chosen (Figure B.8), connected directly to the AC line and using separate rectifier. This power supply at startup turns on the dsPIC and supplies stable 12V for the gate drivers. When the dsPIC has stabilized and performed the initializations a relay is triggered to connect the converter to the line voltage.

The flyback transformer has two secondary windings, one is rated for 12 V output and the other one for 5 V. Only the 12 V output is controlled. This voltage is measured and fed back to the controlled switch. The dsPIC needs an additional 3.3 V voltage stabilizer (*LM1117DT-3.3*) to obtain sharp $VDD = 3.3$V. This additional small supply converter introduce losses of 1.5-2 W.

On the secondary side a 15 V voltage stabilizer (*MC78L15ACDG)* from the output voltage supplies the gate drivers of the synchronous rectifiers.

4.2.6 Discussion

The 600W power supply with interleaved boost PFC converter and phase-shifted full-bridge DC-DC converter with synchronous rectification and current doubler was designed and built in the university laboratory (Figure 4.52).

Figure 4.52: *The 600W power supply*

After testing that the converter power modules, the sensors and the auxiliary power supplies work properly, the measured data had to be analyzed. For this a test firmware was written, which reads the analog channels, transforms them into numerical values with 10 bit analog-to-digital converter and sends them back through the UART channel of the dsPIC. The values were read and plotted in Matlab (Figure 4.53).

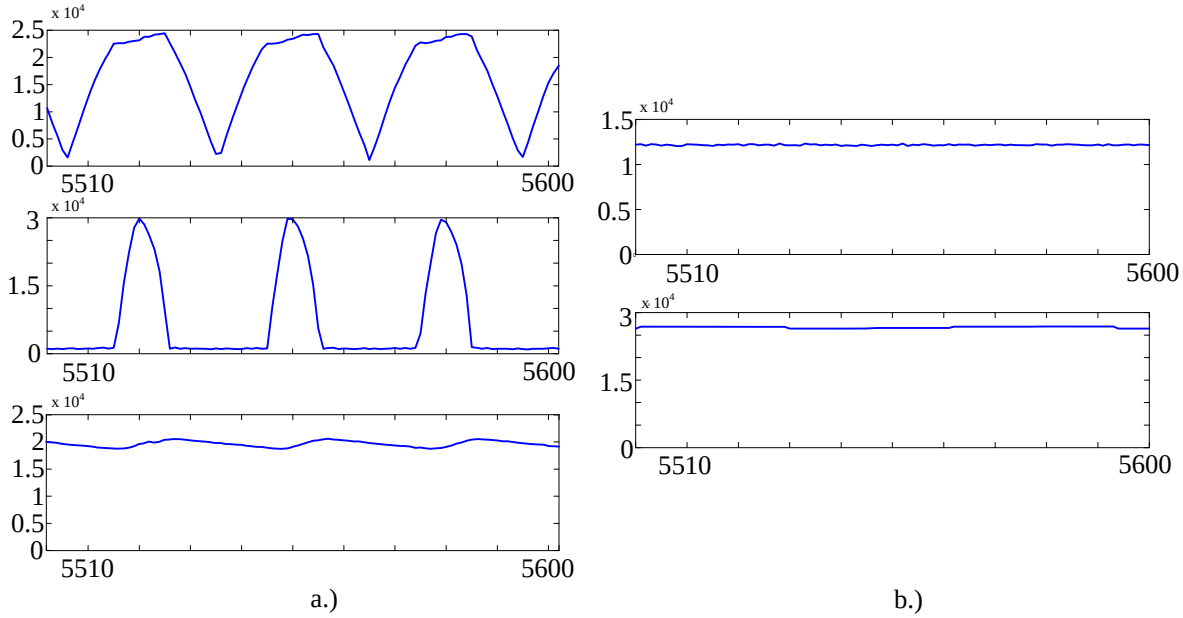
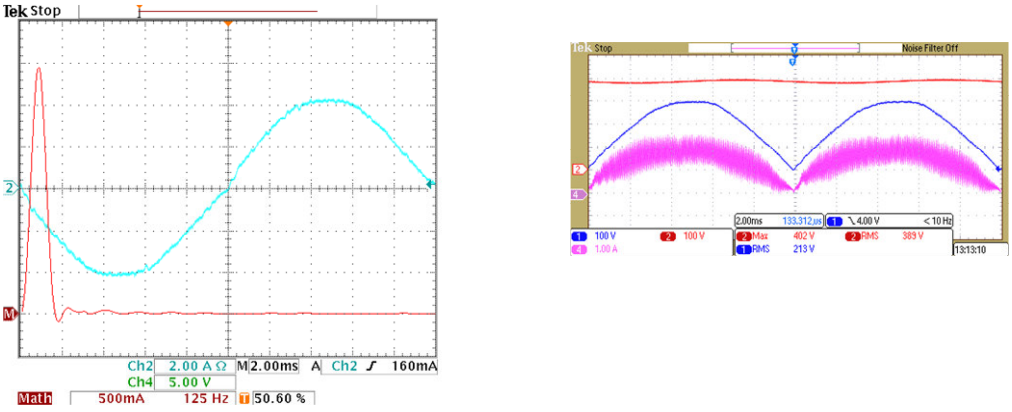


Figure 4.53: *Sampled data in numerical form sent back from dsPIC to Matlab: a.) Interleaved boost waveforms: Top - rectified line voltage, Middle - uncontrolled inductor current, Bottom - uncontrolled DC link voltage; b.) PSFB waveforms: Top - sum of the filter inductor currents, Bottom - uncontrolled output voltage*

The purpose of this test was to start up the converter in open loop, with fixed duty cycle, measure and calibrate the control and measured variables according to the rules of the Q.15 arithmetics. In the dsPIC the sampled values are saved in Q.15 format and represented as 16 bit fixed point signed integers. Thus only the first 11 bits are used: 1 sign bit and 10 data bits. The scale is between [-32768,32767]. As the measured values are positive voltages for measurements the upper [0,32767] interval is used. As shown in Figure 4.53 the interleaved boost and PSFB waveforms are scaled according expectations. Figure 4.53 a.) presents the boost waveforms without PFC and control. Figure 4.53 b.) shows an example for the measured waveforms of the PSFB converter in open loop, fixed duty cycle. The sum of the inductor currents is a numerical value, 12000, which corresponds to 11A. The output voltage is roughly 26000, which corresponds to 35V. All this calculations were done based on the HALL sensor's and voltage divider's gains and the calculations of the analog to digital conversion (3.3V corresponds to 32736 in Q.15 format).

When all the measurements were ready for the control algorithm, all the small measurement amplifiers were scaled to meet the requirements, the two control interrupt routines were loaded to the microcontroller. Firstly, the interleaved boost converter was stabilized as shown in Figure 4.54. The referred figure shows the waveform at full power. The line current is sinusoidal (a.)) with RMS value of 2.9A. The total current harmonic distortion was $THD \leq 4\%$, measured with a PM100 single phase power analyzer. It is in phase with the line voltage (b.)). The two boost inductors share identically half of the line current. The output voltage is controlled to be 390V and has a 100Hz ripple and 5V amplitude. The efficiency and power factor of the interleaved boost converter is shown in Figure 4.55. The power factor is over 0.95 at low power level (50W) and it is 0.996 at full power. The efficiency is 94.3% at full load, but as shown, it is 84% at low power output (50W).



a.) b.)

Figure 4.54: *600W interleaved boost converter waveforms: a.) Cyan - sinusoidal line current, Red - harmonic content of the line current; b.) Blue - rectified line voltage, Pink - interleaved boost inductor current i_{L1}, Red - interleaved boost capacitor voltage*

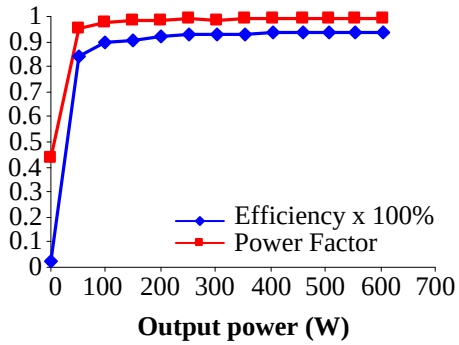
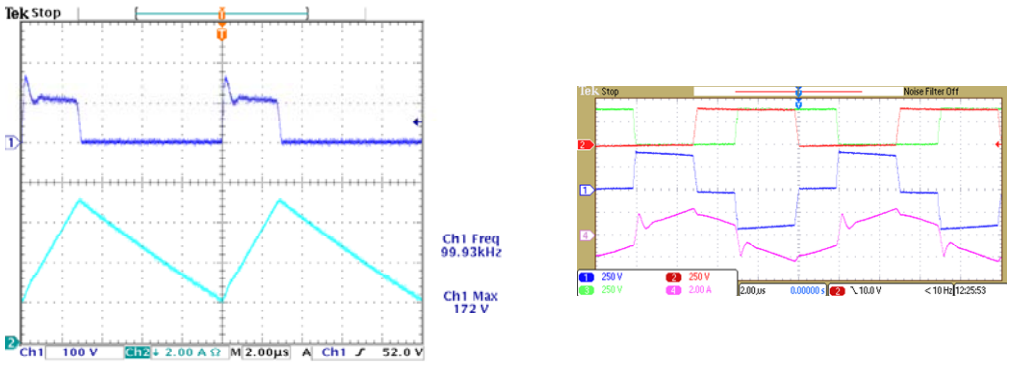


Figure 4.55: *Measured efficiency and power factor of the interleaved boost converter*

Secondarily, the control algorithms for the PSFB converter were implemented in the dsPIC. Figure 4.56 presents the measured waveforms of the phase-shifted full-bridge converter. As it has a current doubler the filter inductor current is half the output current (a.)) Also the drain source voltage of the synchronous rectifiers (SR1 and SR2), though switched with 50% of the switching period duty cycle, it is determined by the phase shift. As it can be seen, to obtain 35V output voltage, around 35% phase shift is required. In the Figure 4.56 b.), the drain source voltages of two opposite leg MOSFETs are presented. The overlap between them (35% of the switching period on $2\mu s$ scale) determines the voltage in the transformer. The Zero Voltage Switching is obtained and it is visible on the transformer currents. While there is voltage on the transformer the current is rising. When the voltage is 0V, the current is decreasing, with the speed determined by the voltage drop on the filter inductors. When the voltage suddenly rises from 0V to the input voltage level, there is a finite slope in the current, determined by the leakage inductance of the transformer. As shown in Figure 4.56, measurement waveforms match the simulated ones (Figure 4.46), which means that a good estimation of the real converter losses and parasitic elements was made and simulated.

The efficiency of the PSFB converter is shown in Figure 4.57. The low efficiency can be explained with transformer and inductor losses. The magnetic components were designed with the goal of reducing the size of them and were built in laboratory.

The overall efficiency of the power supply is close to 85%.



a.) b.)

Figure 4.56: *600W PSFB waveforms a.) Blue - drain-source voltage on one synchronous rectifier SR1, Cyan - filter inductor current i_{Lf1} b.) Blue - Voltage on the primary side of the transformer, Red - drain-source voltage on QA, Green - drain-source voltage on QD, Pink - current in the primary winding of the transformer*

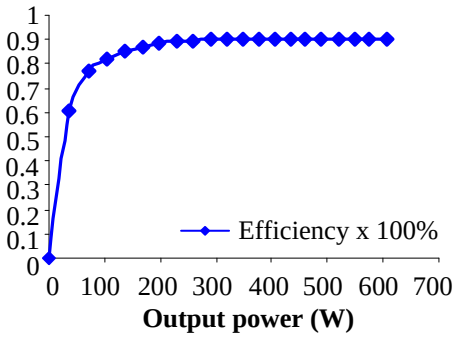


Figure 4.57: *Measured efficiency of the PSFB converter*

4.3 Summary

Digital control in two different application was presented in Chapter 4. Two case studies were conducted and summarized. The first one was a 70 W power supply, using boost PFC and RCD-clamped forward converter DC-DC converters. Based on design requirements the two converters were described. The current and voltage control loops of the boost converter were designed based on the small signal transfer functions. The output voltage control with TL431 shunt regulator and peak current control of the forward converter using the fast analog comparator of the dsPIC was described. Simulation results obtained

from the large signal model and control algorithm, built in Maltab/Simulink using embedded PLECS library, were presented. The designed auxiliary power supply solution was presented which gives the supply voltage for the microcontroller and the gate drivers. The implementation of the hardware and digital controller, firmware challenges and obtained results were presented and evaluated. Finally an identical 70 W power supply was built and tested with a combo analog PFC/PWM controller. The two set of results were compared and evaluated.

A second prototype of 600W two-stage power supply was built. The PFC converter was an interleaved boost and the isolated DC-DC converter was a phase-shifted full-bridge converter with synchronous rectification and current doubler. As it can be seen an increased number of switching components had to be driven at the same time and a microprocessor with higher calculation power was needed to obtain a proper operation. In total 8 PWM channels and two interrupt routines for the two set of current and voltage control loops were used. Digital PI controllers were designed for the interleaved boost converter (current and voltage loop), a digital PI controller for the current loop and a digital PI and fuzzy controller for the PSFB voltage loop. The results with PI and Fuzzy controller were compared and evaluated.

Chapter 5

The influence of grid disturbances on switched-mode power supplies

The following chapter will present an analysis of different grid disturbances, will describe some limitations and immunity requirements based on standards for devices connected to low voltage grid and will show the behavior of digitally controlled boost PFC converter in case of voltage sags.

The input voltage disturbances are translated in the LED current if only one converter is used as LED driver. Thus the light emitted by the LED will contain this variations. To control the LED current and the line current at the same time, intermediate converters with stable DC link voltage are needed. The line connected converter has to reject the effect of the line disturbances and provide the stable DC voltage.

The increased demand for using the power supply network many times ends up in different unwanted events. These industrial events like starting-up of large electrical motors, faults in electrical devices (short circuit drawing high current) or even natural conditions like animals or bad weather (lightning strikes) can cause different deviations of the normal operation of the power supply network. Several power quality disturbances regarding the line voltage are described in IEC 61000-2-1 standard [117],[118]:

- Voltage fluctuation
  Repeated voltage changes. This phenomenon is usually present in the system if devices like welding machines, arc furnaces, etc. are connected to the supplying grid. The amplitude is not exceeding $\pm 10\%$ so most of the equipment are not sensitive to it. However at some devices (CRT televisions and lighting equipment) it can cause visible changes from the normal operation.

- Voltage dips and short supply interruption (*voltage sag*)
  Changes in the RMS value with more than 10% of the voltage for a short period - from half cycle up to 1 minute. The effect of voltage dips is visible in extinction of discharge lamps, failure of computers, speed variation in motor applications.

- Frequency variations
  Deviation from the line frequency is related to changes in the generator frequency.

Many research has been done on the effect of these disturbances on the industrial equipment [123]-[125] but very few work has been presented on the effect of disturbances on office and household single phase devices [126]-[129]. The most common disturbance and most affective on electrical devices from customer point of view is the voltage sag. Different standards exist to meet better power compatibility. The IEC 61000-3-3 [9] limits the flickers and voltage fluctuations impressed by low-voltage line connected equipment. IEC 61000-2-2 [119] and IEC 61000-2-8 [120] gives compatibility levels for trouble free operation of devices connected to public low-voltage supply systems regarding the above mentioned disturbances. Standards SEMI E10-0304, SEMI F47-0706 defines the voltage sag immunity levels for devices connected to single phase low voltage line [121] [122].

The following analysis will focus on voltage sags and their effect on line connected switched-mode power-supplies, especially how is the PFC converter handling the fault events.

5.1 Need for immunity to line disturbances

Concerning electromagnetic compatibility of the line connected electric devices there are two major requirements: firstly the emitted disturbances into the electromagnetic environment should be kept below a limit described by different standards like [7]-[9]. Secondly all equipment connected to the grid should have a certain immunity to disturbances enumerated [118]. These immunity levels are defined in standards like [119]-[121]. The compatibility levels were built up in such way that makes a close coordination between immunity and emission.

The most unpredictable disturbances are the voltage sags and short supply interruptions and they appear with different intensity. Voltage sags are caused by different fault events in line connected equipment, atmospheric phenomena (lightning strike), mechanical contacts (car accidents, excavating machines), animal contacts (squirrels or birds shorting the overhead power lines) or simply aging of the electrical system. During such events high current is drawn for a short time from the voltage source. This is not a regular operation thus it creates irregularities also in the line voltage. The gravity of the effect of the voltage sags not only concentrates on the device itself but the environment it is used. If one device in a production line crashes due to voltage disturbances the whole chain is effected [120]. In hospitals where machines are responsible for human lives, voltage sags or interruptions can have even harder effect than material damage. Immunity to line distortion is essential to reduce material damage or even protect human health or life (medical equipment - EN 60601-1-2, "EMC for Medical Devices").

To describe a voltage sags two parameters are used: the depth of the sag and duration. Most voltage sags last between half a period and one 1 s. Standard [121] and [122] defines a clear classification of voltage sags considering their depth and determines the immunity level for different sag depths in form of duration in time.

The Computer and Business Electronic Manufactures Association (CBEMA) recently called Information Technology Industrial Council (ITIC), name changed to represent a wider group if the industry, has created an envelope of voltage tolerance for computer and other electronic equipment (Figure 5.1). The graph presents the permissible voltage dip expressed in per units in function of duration time. One cycle lasts 20 ms in a 50Hz

system. The line connected devices should resist to a voltage dip of 100% of the line voltage for one period, a voltage dip of 30% of the line voltage for 500 ms, a voltage sag of 20% of the line voltage for 10 s and voltage sag of 10% of the line voltage for more than 100 s. There are limitations for not only voltage drops but also for over voltages. Immunity to over voltages of more than 40% of the nominal line voltage should be up to 3 ms, to over voltages of 20% of the line voltage up to 500 ms and to over voltages up to 10% of the line voltage it should be more than 100 s.

The immunity of IT and process control equipment to voltage sag within the envelop presented on the ITIC figure. As the voltage sags are unpredictable events they can be described only in statistical terms.

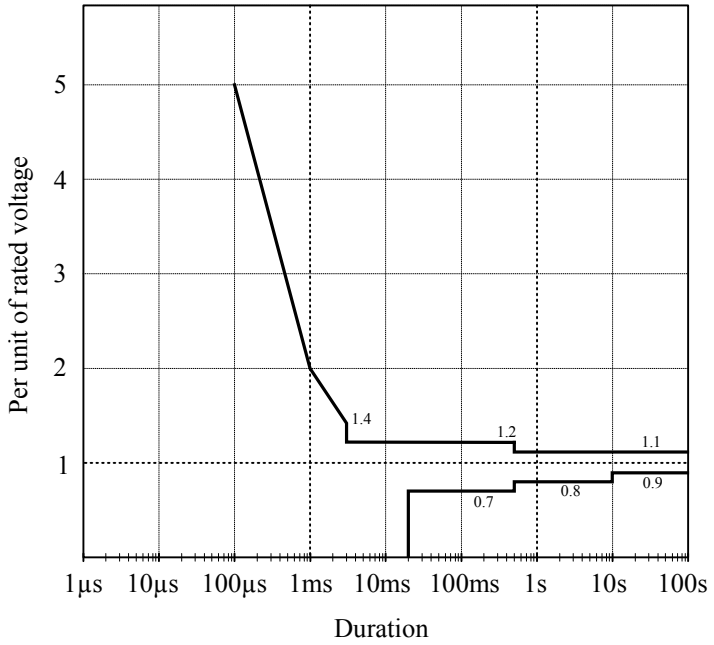


Figure 5.1: *ITIC (CBEMA) voltage sag immunity curves [120]*

A refined version of these recommendations appear in [121], introduced by Semiconductor Equipment and Materials International (SEMI), shown in Figure 5.2. An additional step was included compared to ITIC curves for immunity to a voltage sag of 50% of the line voltage up to 200 ms. It also does not require that devices tolerate voltage sag of 100% for one cycle and voltage sags of 20% of line voltage for more than 1 s.

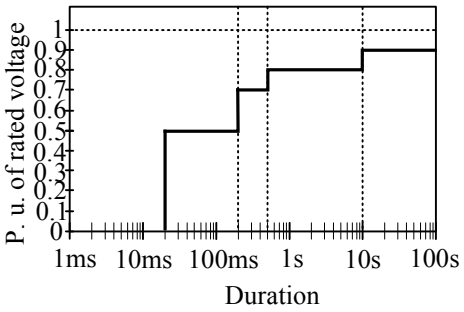


Figure 5.2: *SEMI E10 voltage sag ride-through curvesc [130]*

Immunity to short interruption of the line voltage is not an appropriate concept because no equipment can continue to operate in absence of the supply. Alternatives like restoration of the energy from another supply or development of safe shut-down mechanism have to be planned and implemented.

5.2 Immunity of the digitally controlled boost PFC converter

A solution to provide immunity for line connected switch mode power supply to voltage sags and other disturbances like notches is to apply a power factor preregulator. This not only solves the problem of current shaping but provides a constant DC voltage even in line voltage fault conditions. The investigation was done on a digitally controlled boost PFC convert with a 16 bit fixed point dsPIC microcontroller, so in the followings a brief analysis of the converter and digital control behavior will be presented.

The main focus in this section is on the voltage controller. The current controller dynamics were evaluated in the previews section by presenting the PFC and current THD results. The voltage controller provides amplitude and together with the input measured line voltage determine the reference current. As the effective value of the measured rectified input voltage is use, the amplitude of the current reference would be influenced in case of voltage drops. Another limitation considers the dimensions of the working registers. The 16 bit fix point processor using Q.15 arithmetics limits the processing time and also the scalability of the measured and reference values.

To keep approximately constant the amplitude the waveforms corresponding to the measured input voltage, the maximum of it was measured in every period. Also it was measured the possible highest and possible lowest amplitude of the line voltage. These values were sampled in with 10 bit ADC and the results were 16 bit unsigned integers. The difference between low line and high line maximum, measured with the presented design parameters (sensors, amplifiers, scaling factors, ADC, Q.15 transformation, 16 bit unsigned integer) was around 14000, a number seen inside the microprocessor. Knowing this, a coefficient K was introduced: $K = V_{max} - 14000$, where V_{max} is the amplitude of the sampled line voltage, expressed as an unsigned integer and the constant value is the difference between the high line and low line maximum in Q.15 format. K can also be interpreted as Q.15 number and be used in Q.15 arithmetics like multiplication.

By multiplying according Q.15 arithmetics each sampled voltage value with $Q.15(1) - K$ a unified rectified sinusoidal waveform can be obtained. At low line voltage K is approximately 0 so the multiplication factor is Q.15(1) else it is reduced with K. Also saturation of the voltage controller output is defined by K: $d_{vmax} = ADC_{max} - K$, where ADC_{max} is the maximum value of the 10 bit ADC in signed Q.15 format. Thus high line voltage results in lower current amplitude and for low line voltage the controller will generate high current reference.

Simulation results of the controller behavior to line voltage disturbances are presented in Figure 5.3. Figure 5.3 a.) shows a voltage sag of 50% of the line voltage for 200 ms - according to [121]. In the line current it is visible the effect of the K. In the first half period it starts to drop but after measuring the maximum, the parameter K is recalculated so the reference waveform becomes identical to the one in case of high line. When the line voltage is back to normal, for half period a high current amplitude is present but after recalculating K, the d_{vmax} is limiting it. The output of the voltage controller in low line conditions saturates to the maximum possible for signed integer ($K \approx 0$). Due to this the current amplitude is limited, thus the output voltage is stabilizing with an offset compared to the reference.

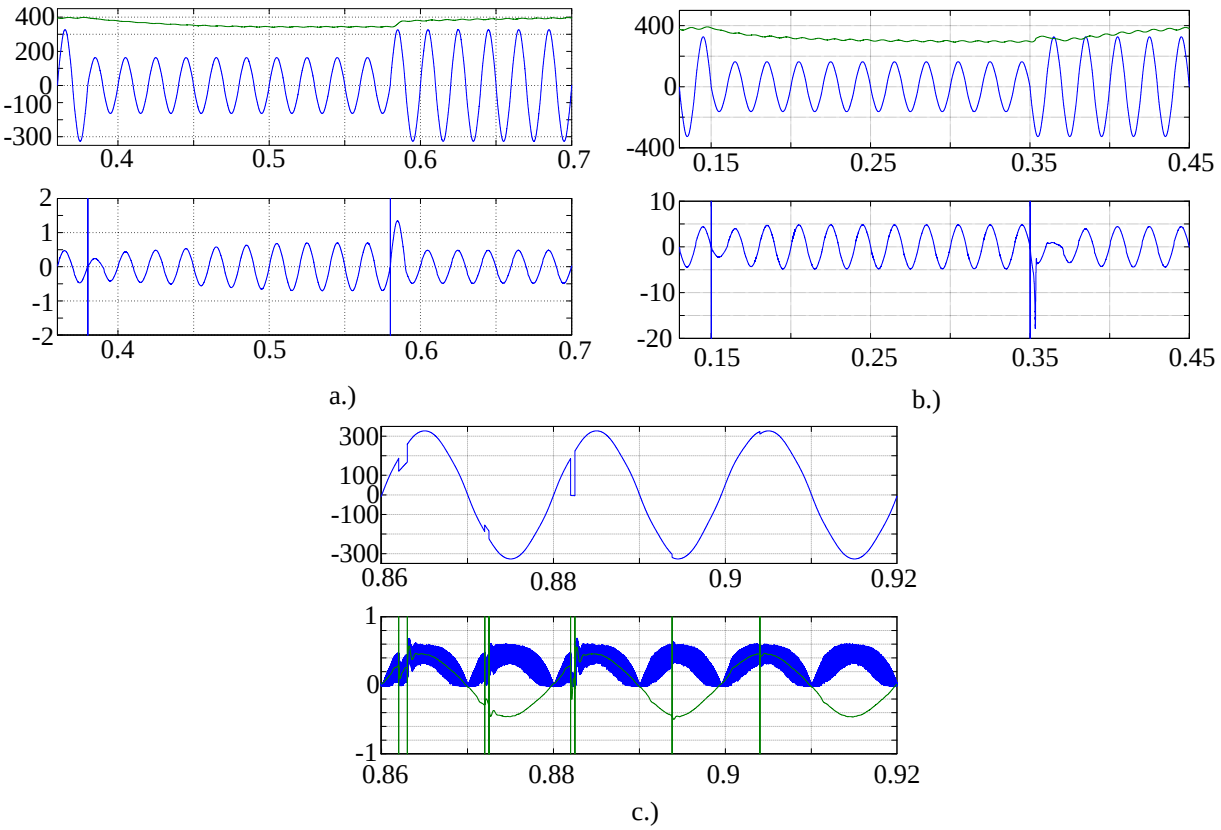


Figure 5.3: *a.) Voltage sag of 50% of the line voltage lasting 200 ms for the 70W converter at nominal power - top: green - DC boost voltage, blue - line voltage, bottom: line current; b.) Voltage sag of 50% of the line voltage lasting 200 ms for the 600W at nominal power - top: green - DC boost voltage, blue - line voltage, bottom: line current; c.) Notches in the line voltage - top: line voltage, bottom: green - line current, blue - boost inductor current*

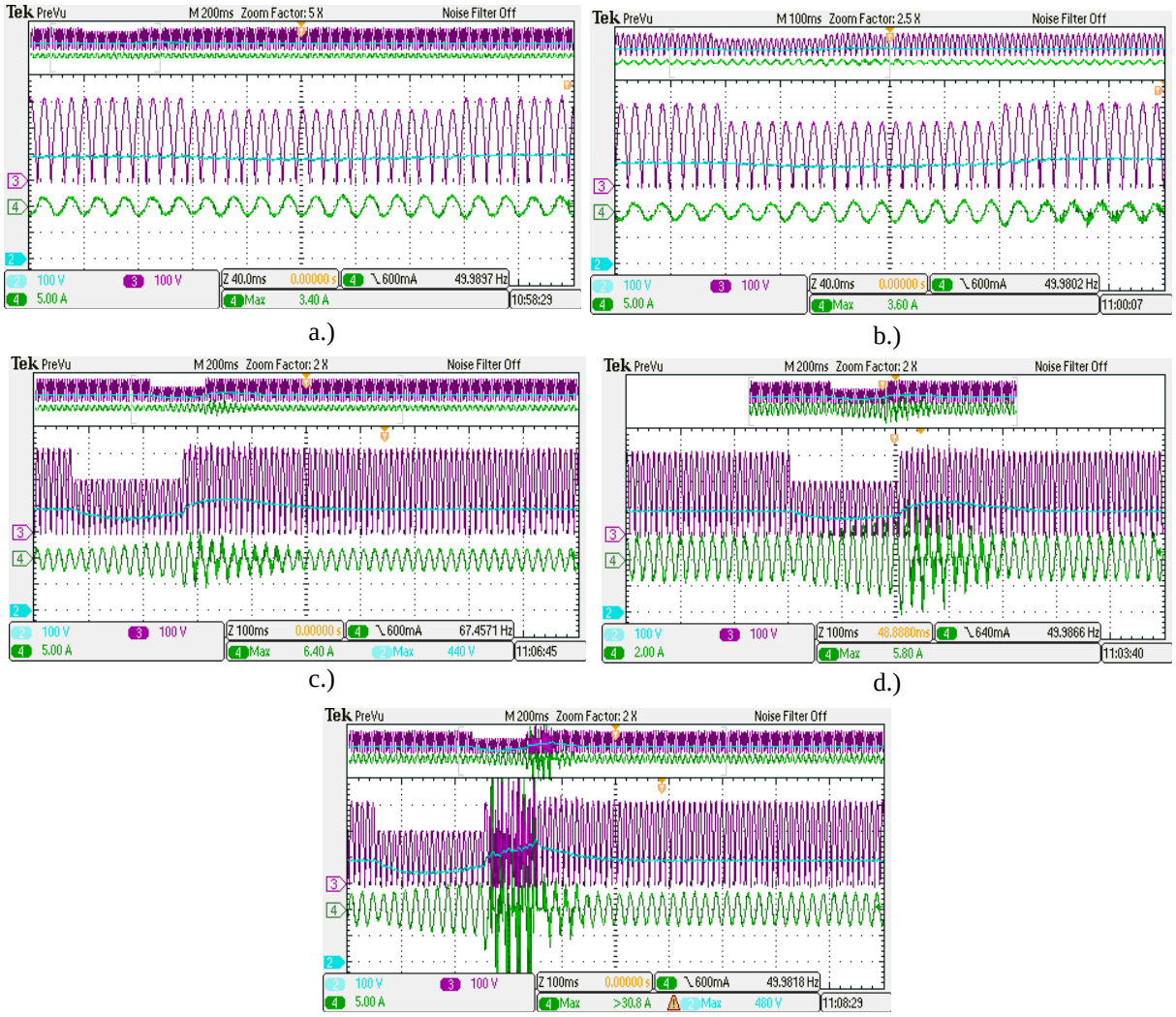


Figure 5.4: *Cyan - DC boost voltage, purple - rectified line voltage, green - line current; a.) Voltage sag to 200V from 230V of the line voltage lasting 200 ms at 250W b.) Voltage sag to 180V from 230V of the line voltage lasting 200 ms at 250W; c.) Voltage sag to 150V from 230V of the line voltage lasting 200 ms at 250W; d.) Voltage sag to 150V from 230V of the line voltage lasting 200 ms at 350W; e.) Voltage sag to 150V from 230V of the line voltage lasting 200 ms at 450W.*

The control was tested also on a simple digitally controller boost converter (Figure 5.3 a.)) with 70W output power. In case of the high power, 600W version (Figure 5.3 b.)), when the line voltage reentered to the normal operation, the current limitation was visibly turned on reducing d_{vmax}. One solution to prevent the converter and the load from damaging is to have a strong voltage control loop with stronger controller to maintain the DC link voltage at the required level during AC voltage drop. In the presented design a faster processor could be used with higher processing capability. Thus a PLL loop could be implemented based on the line voltage fundamental frequency. This would give the reference waveform to the line current and it would be less dependent and affected by the line voltage variations. By overrating the power supply, the voltage controller will also be

less likely to saturate. Figure 5.3 c.) presents the current response to different events like notches or phase jump. As the current controller has high bandwidth close to 10 kHz, it is following the smallest deviation in the current reference.

Experimental results are presented in Figure 5.4. The interleaved boost converter is part of the 600W two-stage PFC/DC-DC converter presented in Chapter 4.2. The digital controller is supplied (3.3V) by a small flyback converter which is connected directly to the ac line. This requires a minimum of 130V to turn on. Thus voltage sag with maximum voltage drop from 230V to 150V could only be tested with the presented design. When dropping under 130V, the dsPIC simply turned off and the converter started behaving as a non-controller diode rectifier connected to the load. As the line voltage stabilized back in the normal operation range, the controller could be restarted with a reset button. Experimental results are presented for different level of voltage sags with different power levels. In the following figures the magenta color is the rectified line voltage, the green is the line current and the cyan is the boost DC voltage. The applied voltage sag lasted ten line periods in each measurement (200ms at 50 Hz line).

As shown in Figure 5.4 a.) the drop is only 30V thus the line current and voltage is not influenced much. In Figure 5.4 b.) the voltage dropped to 180VAC. When it stabilized to normal operating conditions, the line current got a sudden high reference value which drove it into over current mode and the controller turned on the current limitation by reducing the duty cycle maximum limit. With this for short time spikes appear in the line current. The amplitude of the spikes is load dependent (as visible on the later figures). In Figure 5.4 c.) voltage sag of 150VAC is presented. The bigger the amplitude of the sag, the larger stabilizing time was needed for the output voltage and line current. As shown in Figure 5.4 d.) the load was changed to 350W for voltage sag of 150VAC. The higher the load the lower the output voltage dropped and the longer the transient period lasted to stabilize the dc voltage and ac current after reentering in the normal line operation. On this figure it is clearly visible the effect of the peak detection. At the first half period of the voltage sag the current followed the low reference. After peak detection the current reference waveform was recalculated with the factor K presented in the section III. A. When reentering the normal mode the reference amplitude is still high; in the first half period high line current is visible. The second it detected the new peak, the K was recalculated and the new reference was determined. The last figure (Figure 5.4 e.)) presents the voltage sag to 150VAC with 450W. The current limiter introduced large sparks in the system as the load required input power. So this solution is not so effective at high power levels and the possibility of other faults due to high current stress persists there.

The work in this chapter is summarized in the paper "Effect of voltage sags on digitally controlled line connected switched-mode power supplies" presented on the International Conference on Optimization of Electrical and Electronic Equipment - OPTIM 2012, Brasov, Romania.

5.3 Summary

Different voltage disturbances, grid codes and standards which ensure immunity for low-voltage line connected devices in case of line disturbances were presented in this chapter. Also the behavior of the line connected PFC converter and the dynamics of its digital

controller was analyzed in case of voltage sags. This is important because it has the responsibility to supply the second stage with a fixed DC voltage or turn off the converter in case of critical faults. Results were evaluated and solutions were proposed to improve the performance.

Chapter 6

Conclusions

Switched-mode power-supplies have been used for several decades to supply the different low-voltage line-connected devices. These loads have highly nonlinear characteristics and draw non-sinusoidal line current. Regulations for EMI have made necessary to introduce current shaping circuits to reduce the harmonic content of the line current and increase the power factor. A brief description of the standards which limit the current harmonics and voltage disturbances impressed by the low-voltage line connected devices was presented in the beginning of the thesis. After describing, how to determine the THD and power factor analytically from non-sinusoidal voltage and current waveforms, different power factor corrector techniques and DC-DC converter topologies for different power levels were described, fulfilling the first objective of the work.

In power factor correction techniques major focus was on active solutions and within this the boost converter-type converters and their operation modes were discussed in details. Advantage of the boost converter in power factor correction is that it is simple and by construction it is ideal for current shaping. Its disadvantage is the lack of inrush current control on the main current path and the high output voltage. Interleaving techniques are used for boost converters at high power levels to reduce the current stress on the switching devices and the size of the boost inductor. Disadvantage is the increased number of magnetic and switching components.

To obtain the required load voltage a second-stage step down converter is required. Different buck-derived topologies exist according to the required power level. Isolated topologies were mainly discussed so this way galvanic isolation between the load and the line is obtained. Brief description of the EMI filter and filter design was also presented.

Different challenges and requirements were presented in this chapter in order to design a digital controller. Firstly the effect of sampling and PWM resolution, aliasing effect and proper bandwidth selection are analyzed. To reduce sampling and PWM errors high resolution analog-digital converters (10bit) and PWM modules (13 bit) were chosen. The highest frequency for inductor current sampling was 50kHz, half of the switching frequency. The voltages were sampled either with 10 kHz for boost DC-link voltage either with 5 kHz for PSFB output voltage. These frequencies serve for low bandwidth voltage control loops.

Afterwards the small signal model of the boost, interleaved boost and PSFB converters was built, the required transfer functions were obtained and discretization was performed

with Bilinear transformation method. It was shown that the small signal models of the boost converter and interleaved two-leg boost converter are almost identical. The only difference is that in case of interleaving the boost inductor is replaced with the paralleled inductors from each leg. The model is valid if the sum of the inductor currents is controlled. The PSFB converter with synchronous rectification and current doubler can be modeled as an interleaved synchronous buck converter, making the controller design easier. The model is valid if the sum of the filter inductor currents is measured and used as control variable. The most commonly used controller in power electronics is the PI controller. Digital implementation of it is discussed, using Bilinear transformation for discrete integral. Thanks to the digital solution an alternative to the PI controller, a nonlinear solution can be applied. The fuzzy control method is introduced and discussed as high frequency voltage control solution. Thus second objective of the thesis is discussed.

To validate the feasibility of digital control for switched mode power-supplies, two case studies were conducted and summarized. The first one was a 70 W power supply, using boost PFC and RCD-clamped forward converter DC-DC converters. Based on design requirements the two converters were designed. The large signal boost converter model was built in in Matlab/Simulink using embedded PLECS library. To control the inductor current and DC voltage, a Simulink model was designed, built and tested. The required dsPIC operations were emulated in the model. The control algorithms were programmed in a triggered embedded Matlab function. This works like the ADC interrupt of the microcontroller and gives the duty cycle value for the PWM generator. The PWM signals were also generated by a triggered embedded Matlab function, using a counter to define the ramp for the carrier wave. The resolution of the PWM was reduced to 7 bits, the half of the real resolution to reduce the simulation time. This generator also ensured the triggering of the control function block in the middle of the ON time of the switching MOSFET. With this sampling pattern the average current value was obtained. The same control code and controller parameters were programmed in the dsPIC and simulation results were compared to the measured one.

The output voltage is controlled by a TL431 shunt regulator and the current limitation is obtained by a peak current controller in the forward converter using the fast analog comparator of the dsPIC. To drive microcontroller and external gate drivers an auxiliary power supply was needed. Different solutions were presented and the final version was discussed in details. These additional hardware elements increased a little the over-all price of the power supply and also resulted in a small drop in efficiency.

An identical 70 W power supply was built and tested with a combo analog PFC/PWM controller. The results obtained from the digitally and analog-controlled converters were compared and evaluated. As results and hardware comparison showed, digital control can be competitive with the analog one in terms of power factor and efficiency. Digital results showed lower efficiency which is the result of the additional power supply and due to the small differences in the forward transformer design. The economic reasons for using digital control is not clear compared to the prices of the dedicated integrated analog controllers. On the other hand, with falling prices of microcontrollers and increasing demands on the performance of power converters introducing digital control seems to be a reasonable option for the future development of power converters. The opportunity to realize non-

linear, predictive and adaptive control strategies and monitoring the system behavior provides a strong reason why digital control could yield worthwhile advantages compared with state-of-art analog controllers.

A second digitally controlled prototype of 600 W two-stage power supply was built. The PFC converter is an interleaved boost and the isolated DC-DC converter is a phase-shifted full-bridge converter with synchronous rectification and current doubler. As it can be seen an increased number of switching components has to be driven at the same time and a microprocessor with higher calculation power to obtain a proper operation. In total 8 PWM channels were used and two interrupt routines for the two set of current and voltage control loops. The control algorithms were designed and simulated in Matlab/Simulink environment using the PLECS large signal model of the interleaved boost and PSFB converters. With the proper scaling of the measured values the same control algorithm and simulation platform could be used for both converters as presented in case of the 70 W converter. Digital PI controllers were implemented in the dsPIC for the current and voltage control loop of the interleaved boost and PSFB converters. Also digital a fuzzy controller was designed, simulated and implemented for the PSFB voltage loop. The dynamic response of the voltage loop with PI and Fuzzy voltage controllers was compared and evaluated. With the same controller parameters the fuzzy controller produced better transient dynamics for the output voltage than the PI controller.

Presenting the simulation, measurement and comparison results and work, the third and fourth objective of the thesis was discussed and fulfilled.

The designed and controlled switched-mode power-supplies should meet the regulations regarding immunity to line disturbances. The final part of the work presented different voltage disturbances. To ensure this fault immunity for equipment connected to low voltage supply grids, different grid codes and standards were presented. Based on these standards the behavior of the line connected PFC converter and its dynamics with digital controller was analyzed in case of voltage sags. The first stage of the converter is responsible to ensure the current shaping but also to supply the second stage with a fixed DC voltage or shut down the converter in case of a critical faults. Results were evaluated and solutions were proposed to improve the performance. By this work the last objective of the work is fulfilled.

As the controller is dependent on the line voltage in determining the reference current shape to perform the required power factor correction, PLL loop could be used. Such way the dependency from the line voltage amplitude could be eliminated. To control switch-mode power-supplies with high switching frequency and using a single microcontroller, processors with 16 bit fixed point Arithmetical-Logical-Unit hit some limitations in calculation time. In future the price of floating point DSPs will decrease, thus processors with 32 bit floating point ALU could be used to improve calculation speed and performance.

6.1 Future work

To keep component prices low, cheap microprocessor was used with limited calculation power. More advanced algorithms like implementing PLL to trace better the line voltage, processors with higher processing (with 32 bit fix or floating point ALU) power could be

used and tested.

More advanced digital solutions like FPGAs could be used to embed digital controller to the power circuit. It would give the designer freedom to decide which algorithm with specific input/output requirements should be used. Additional controller losses could be reduced by not supplying the not used modules like it is in case of a usual microcontroller

In absence of echo-less room only conducted EMI test were carried out. To comply with standards radiated EMI test should also be made in the future with the digitally controlled power supplies.

The converter reliability to temperature variation, aging of the components, voltage and current stresses could be checked to get a complete picture about the system from control, EMI and reliability point of view.

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Appendix A

Inductor and transformer designs

A.1 Boost inductor design

The design parameters are the followings:

V_{ac}	85-265 V	Input voltage
Vdc	400 V	Output voltage
Po	70 W	Nominal output power
P_{tot}	$1\% \cdot Po$ W	Total losses in the inductor
η	98%	Efficiency
f_L	40-60 Hz	Line frequency
f_s	100 kHz	Switching frequency
ΔI	$25\% \cdot I_{Peak}$ A	Current ripple
K_u	0.5	Winding fill factor (50%)
ρ	$1.724 \cdot 10^{-6}$ Ωcm	Copper wire effective resistivity
μ_0	$4 \cdot \pi \cdot 10^{-7}$	Magnetic constant

Table A.1: *Boost inductor design parameters*

β	2.6	Core loss exponent for high frequency ferrite material
K_{fe}	20 W/cm^3T^β	Core loss coefficient
B_{sat}	390 mT	Saturation flux for N87 ferrite material

Table A.2: *N87 ferrite material properties*

Ac (cm^2)	Wa (cm^2)	MLT (cm)	lm (cm)	weight (g)
0.98	0.415	5.2	4.4	22

Table A.3: *RM10 core parameters*

The design of the inductor is made based on [10] pp. 565-586.

Having all the input parameters, the required inductance value can be calculated and the maximum duty cycle:

$$I_{Peak} = \frac{Po \cdot \sqrt{2}}{\eta \cdot V_{ac-min}} = 0.61A \tag{A.1}$$

$$\Delta I = 0.25 * I_{peak} = 0.15A \tag{A.2}$$

$$I_{avg} = I_{Peak} - \Delta I = 0.46A \tag{A.3}$$

$$L = \frac{(Vdc - V_{ac-min}) \cdot \frac{V_{ac-min}}{Vdc}}{2 \cdot \Delta I \cdot f_s} = 2.7mH \tag{A.4}$$

$$D = 1 - \frac{V_{ac-min}}{Vdc} = 0.185 \tag{A.5}$$

Cores made of Ferrite material are recommended for high frequency operation. The chosen material type is N87. To determine the perfect core type, first a constant is defined based on the application properties:

$$K = \frac{\rho \cdot \lambda^2 \cdot I_{avg}^2 \cdot (K_{fe})^{\frac{2}{\beta}}}{4 \cdot K_u \cdot (P_{tot})^{\frac{\beta+2}{\beta}}} \cdot 10^8; \tag{A.6}$$

where

$$\lambda = D \cdot \frac{1}{f_s} \cdot V_{ac-min} = 0.84 \cdot 10^{-3} \tag{A.7}$$

is the volt-second of the input voltage during "on" time of the switching transistor. The term 10^8 is compensating and transfers to the basic SI system the parameters given in cm^2. Based on core properties another constant can be defined which looks like:

$$K_{gfe} = \frac{Wa \cdot (Ac)^{\frac{2\cdot(\beta-1)}{\beta}}}{MLT \cdot (lm)^{\frac{2}{\beta}}} \cdot \left[\left(\frac{\beta}{2}\right)^{-\frac{\beta}{\beta+2}} + \left(\frac{\beta}{2}\right)^{\frac{2}{\beta+2}}\right]^{-\frac{(\beta+2)}{\beta}}; \tag{A.8}$$

and this constant should fulfill the:

$$K_{gfe} \geq K \tag{A.9}$$

condition. Considering its characteristics at 100 kHz switching frequency (Table A.2) an RM10 shape core was chosen, which meets the design requirements and fulfills the A.10 condition:

$$7.4 \cdot 10^{-3} \geq 0.242 \cdot 10^{-3} \tag{A.10}$$

Determining the optimum flux density:

$$\Delta B = \left(10^8 \cdot \underbrace{\frac{\rho \cdot \lambda^2 \cdot I_{avg}^2}{2 \cdot K_u}}_{application} \cdot \underbrace{\frac{MLT}{Wa \cdot Ac^3 \cdot lm}}_{core} \cdot \underbrace{\frac{1}{\beta \cdot K_{fe}}}_{material}\right)^{\frac{1}{\beta+2}} = 0.0542 \text{ T} \tag{A.11}$$

The above equation has three parts: one based on application properties, one based on

core type characteristics and one based on the chosen material.

Having defined the optimum flux density, the required number of turns is given by:

$$n = \frac{\lambda}{2 \cdot \Delta B \cdot Ac} \cdot 10^4 \approx 79; \tag{A.12}$$

The required gap length:

$$l_g = \frac{\mu_o \cdot Ac \cdot n^2}{L} \cdot 10^{-4} = 0.28mm; \tag{A.13}$$

To meet design requirements the wire size, which should be used:

$$Aw < \frac{Ku \cdot Wa}{n} = 2.6 \cdot 10^{-3} cm^2; \tag{A.14}$$

Thus the chosen copper wire was the AWG24 with diameter of 0.5 mm and a cross section are of $Aw = 2 \cdot 10^{-3} cm^2$.

The losses in the windings and the core can be calculated as:

$$P_{Co} = \frac{\rho \cdot n \cdot MLT}{Aw} \cdot I_{avg}^2 = 0.0734W; \tag{A.15}$$

$$P_{Fe} = Kfe \cdot \Delta B^{\beta} \cdot Ac \cdot lm = 0.0441W; \tag{A.16}$$

$$P_{tot} = P_{Co} + P_{Fe} = 0.1175W; \tag{A.17}$$

$$\tag{A.18}$$

A.2 Forward transformer design

Vdc	400 V	Input voltage
V_f	14 V	Output voltage
Po	70 W	Nominal output power
P_{tot}	$1\% \cdot Po$ W	Total losses in the transformer
η	98%	Efficiency
f_s	100 kHz	Switching frequency
K_u	0.5	Winding fill factor (50%)
ρ	$1.724 \cdot 10^{-6}$ Ωcm	Copper wire effective resistivity
μ_0	$4 \cdot \pi \cdot 10^{-7}$	Magnetic constant
D_{max}	$30 \cdot \frac{1}{f_s}$	Maximum allowed duty cycle

Table A.4: *Forward transformer design parameters*

The required turn ratio:

$$n = \frac{V_f}{Vdc \cdot D_{max}} = 8.57 \tag{A.19}$$

The applied primary volt-second balance:

$$\lambda 1 = D \cdot \frac{1}{f_s} \cdot Vdc = 0.0012V - \mu s \tag{A.20}$$

The primary rms current:

$$I_{1rms} = \frac{1}{2} \cdot (\frac{n_2}{n_1} \cdot I_2 + \frac{n_3}{n_1} \cdot I_3) \cdot \sqrt{D} = 0.3423A \tag{A.21}$$

where $I_2 = I_3 = 2.5A$ and n_2, n_3 are the number of turns in the secondary winding of the dual output forward transformer. The two secondary windings carry rms current:

$$I_{2rms} = I_{3rms} = \frac{1}{2} \cdot I_2 \cdot \sqrt{1 + D} = 1.425A \tag{A.22}$$

The total rms winding current referred to the primary:

$$I_{tot_rms} = I_{1rms} + 2 \cdot \frac{n_2}{n_1} \cdot I_{2rms} \cdot \frac{n_3}{n_1} \cdot I_{3rms} = 1.0549A \tag{A.23}$$

Similarly to the boost inductor (RM10 core), the forward transformer core size is evaluated based on A.8 and A.9.Thus:

$$K_{gfe} \geq K \Leftrightarrow 0.0074 \geq 0.0026 \tag{A.24}$$

According to A.11 the peak ac flux density is:

$$\Delta B = 0.0908T \tag{A.25}$$

The primary turns are determined by A.12: $n1 = 67$ turns. The two secondary windings are respectively:

$$n_2 = n_3 = \frac{n_1}{n} = 8; \tag{A.26}$$

The copper and core losses are :

$$P_{total} = P_{cu} + P_{fe} = 0.218W + 0.168W = 0.386W \leq P_{tot} \tag{A.27}$$

A.3 Boost inductor design for interleaved PFC converter

The design parameters are the followings:

V_{ac}	85-265 V	Input voltage
Vdc	400 V	Output voltage
Po	600 W	Nominal output power
P_{tot}	$1\% \cdot Po$ W	Total losses in the inductor
η	98%	Efficiency
f_L	40-60 Hz	Line frequency
f_s	100 kHz	Switching frequency
ΔI	$25\% \cdot I_{Peak}$ A	Current ripple

Table A.5: *Interleaved boost inductor design parameters*

The chosen core is a Kool Mu 0077324A7 with the following characteristics:

Ac(mm^2)	67.8
Wa(mm^2)	356.3
MLT(mm)	48
lm(mm)	89.8
weight(g)	37.4
I.D.(mm)	21.54
O.D.(mm)	36.7
Width(mm)	11.35
μ	125

Table A.6: *Kool Mu 0077324A7 core parameters*

A.4 Full-bridge transformer design

The design parameters are the followings:

Vdc	400 V	Input voltage
V_o	35 V	Output voltage
Po	600 W	Nominal output power
P_{tot}	$1\% \cdot Po$ W	Total losses in the transformer
η	98%	Efficiency
f_s	100 kHz	Switching frequency
K_u	0.5	Winding fill factor (50%)
ρ	$1.724 \cdot 10^{-6}$ Ωcm	Copper wire effective resistivity
μ_0	$4 \cdot \pi \cdot 10^{-7}$	Magnetic constant
D_{eff}	$35 \cdot \frac{1}{f_s}$	Maximum allowed duty cycle

Table A.7: *PSFB transformer design parameters*

The required turns ratio:

$$n = \frac{V_o}{Vdc \cdot D_{max}} = 3.42 \tag{A.28}$$

The applied primary volt-second balance:

$$\lambda 1 = D \cdot \frac{1}{f_s} \cdot Vdc = 0.0014V - \mu s \tag{A.29}$$

The primary rms current:

$$I_{1rms} = \frac{1}{2} \cdot (\frac{n_2}{n_1} \cdot I_2 + \frac{n_3}{n_1} \cdot I_3) \cdot \sqrt{D} = 1.59A \tag{A.30}$$

where $I_2 = 9A$ and n_2 is the predicted number of turns in the secondary winding of the dual output forward transformer. The secondary winding carry rms current:

$$I_{2rms} = \frac{1}{2} \cdot I_2 \cdot \sqrt{1 + D} = 5.228A \tag{A.31}$$

The total rms winding current referred to the primary:

$$I_{tot_rms} = I_{1rms} + 2 \cdot \frac{n_2}{n_1} \cdot I_{2rms} \cdot \frac{n_3}{n_1} \cdot I_{3rms} = 4.734A \tag{A.32}$$

The ETD44 core parameters are presented in Table A.8.

Ac (cm^2)	Wa (cm^2)	MLT (cm)	lm (cm)	weight (g)
1.74	2.13	7.62	10.3	94

Table A.8: *ETD44 core parameters*

The PSFB transformer core size is evaluated based on A.8 and A.9.Thus:

$$K_{gfe} \geq K \Leftrightarrow 0.0274 \geq 0.0016 \tag{A.33}$$

According to A.11 the peak ac flux density is:

$$\Delta B = 0.0811T \tag{A.34}$$

The primary number of turns are determined by A.12: $n1 = 50$ turns. The calculated number of turns in the secondary winding is:

$$n_2 = \frac{n_1}{n} = 15; \tag{A.35}$$

The copper and core losses are :

$$P_{total} = P_{cu} + P_{fe} = 0.6797W + 0.5229W = 1.202W \leq P_{tot} \tag{A.36}$$

Appendix B

Schematics

B.1 70 W converter schematics

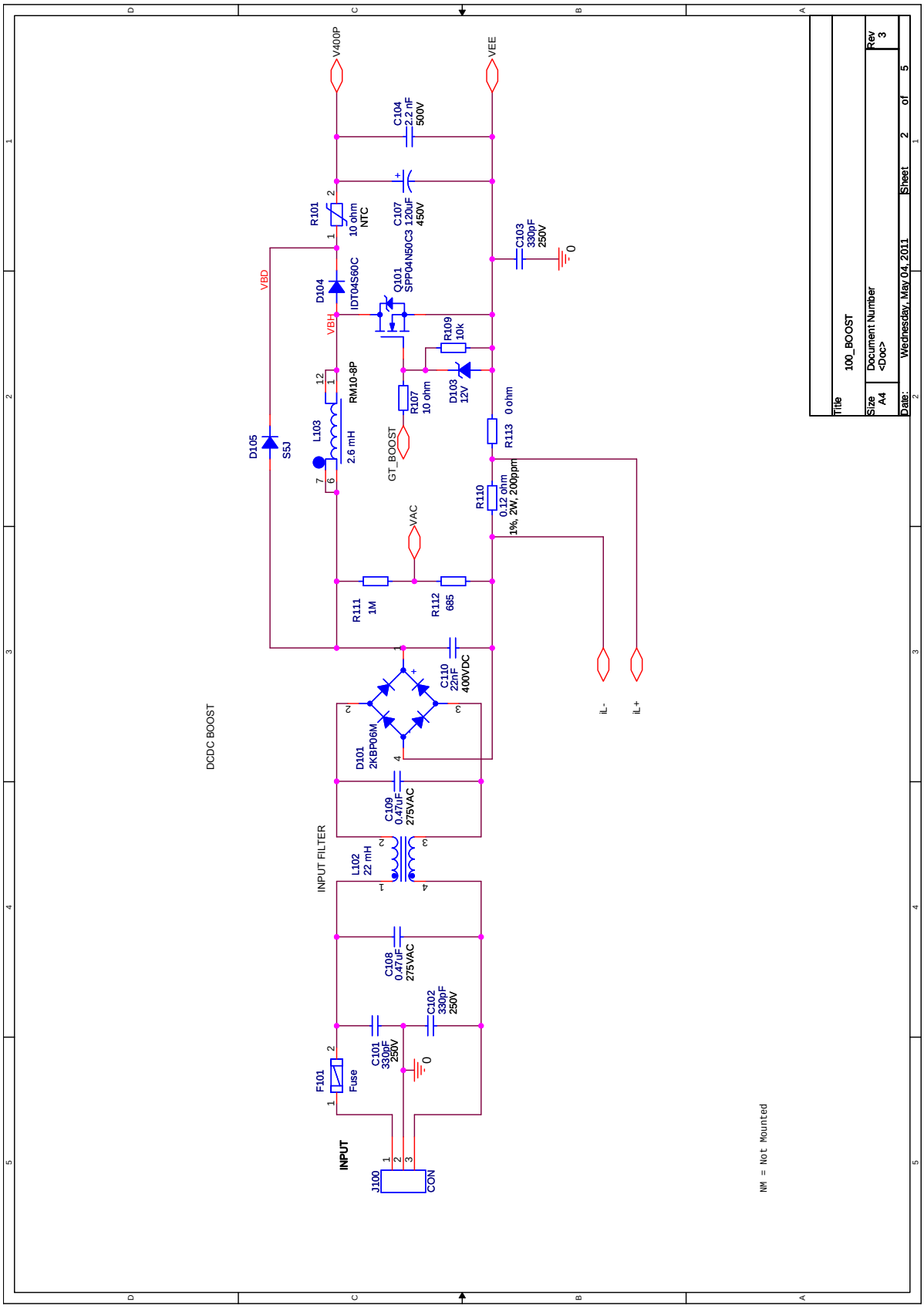

Figure B.1: *Boost converter schematic*

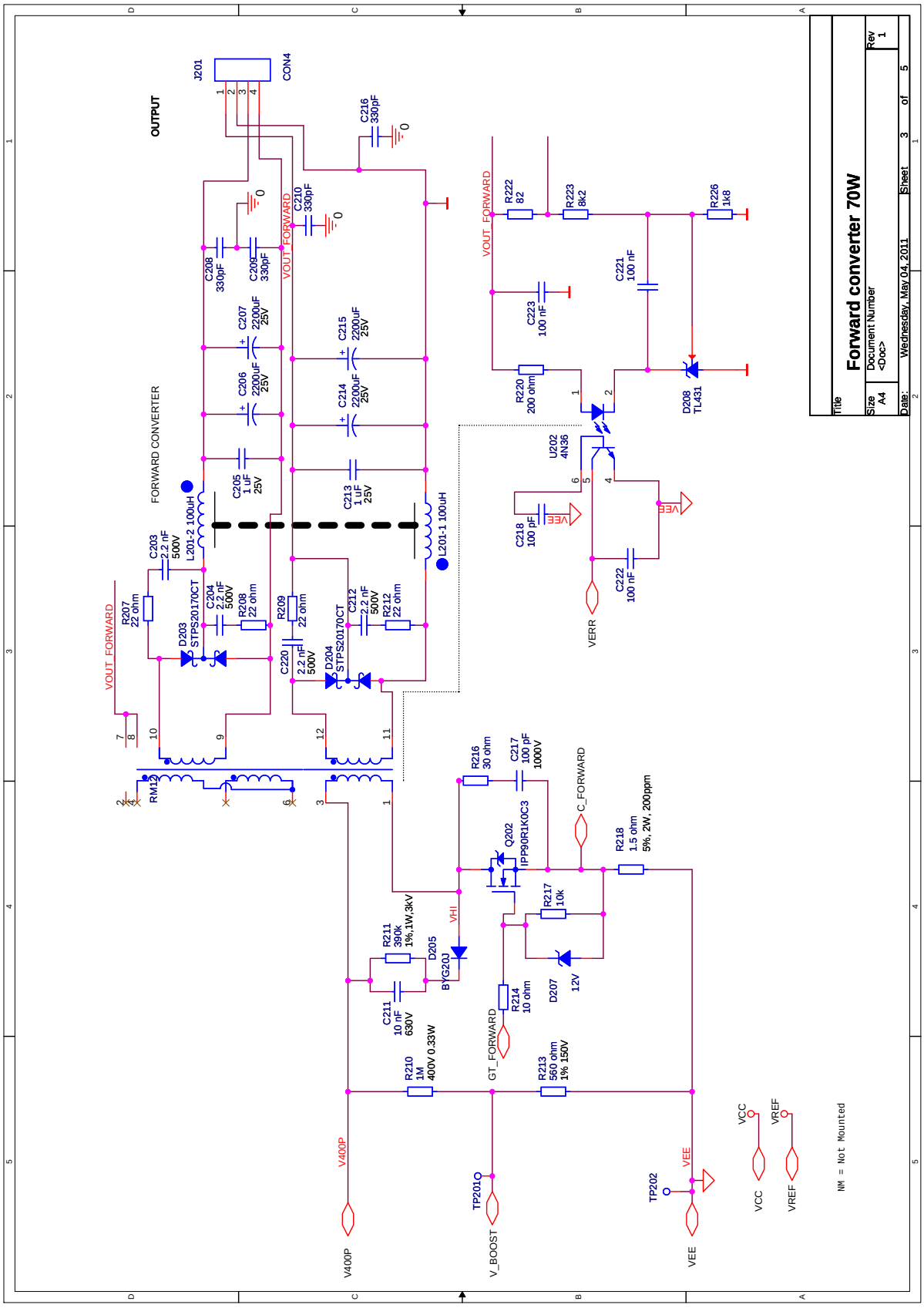

Figure B.2: *Two output forward converter schematic*

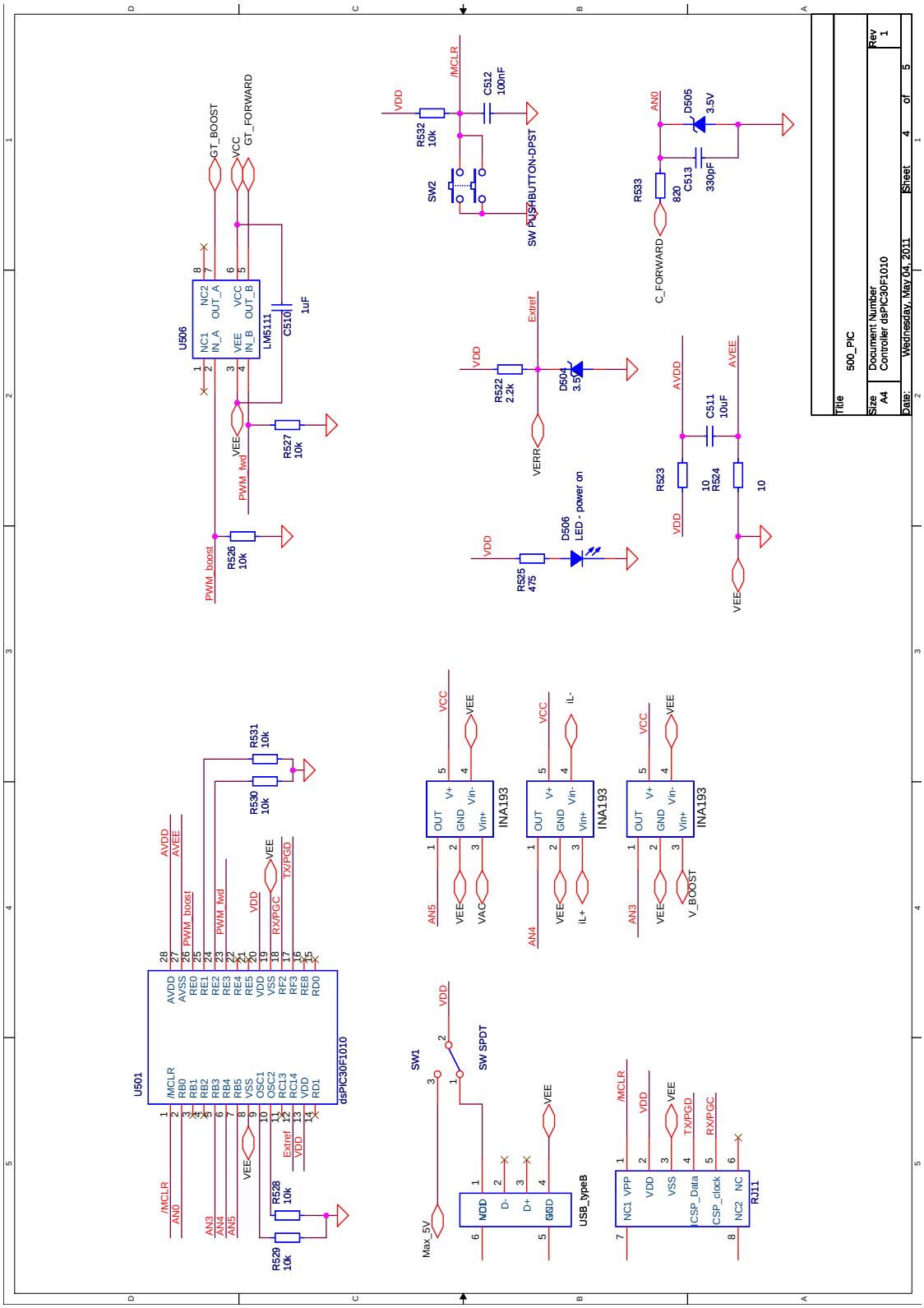

Figure B.3: *dsPIC connections - dsPIC30F1010 - schematic*

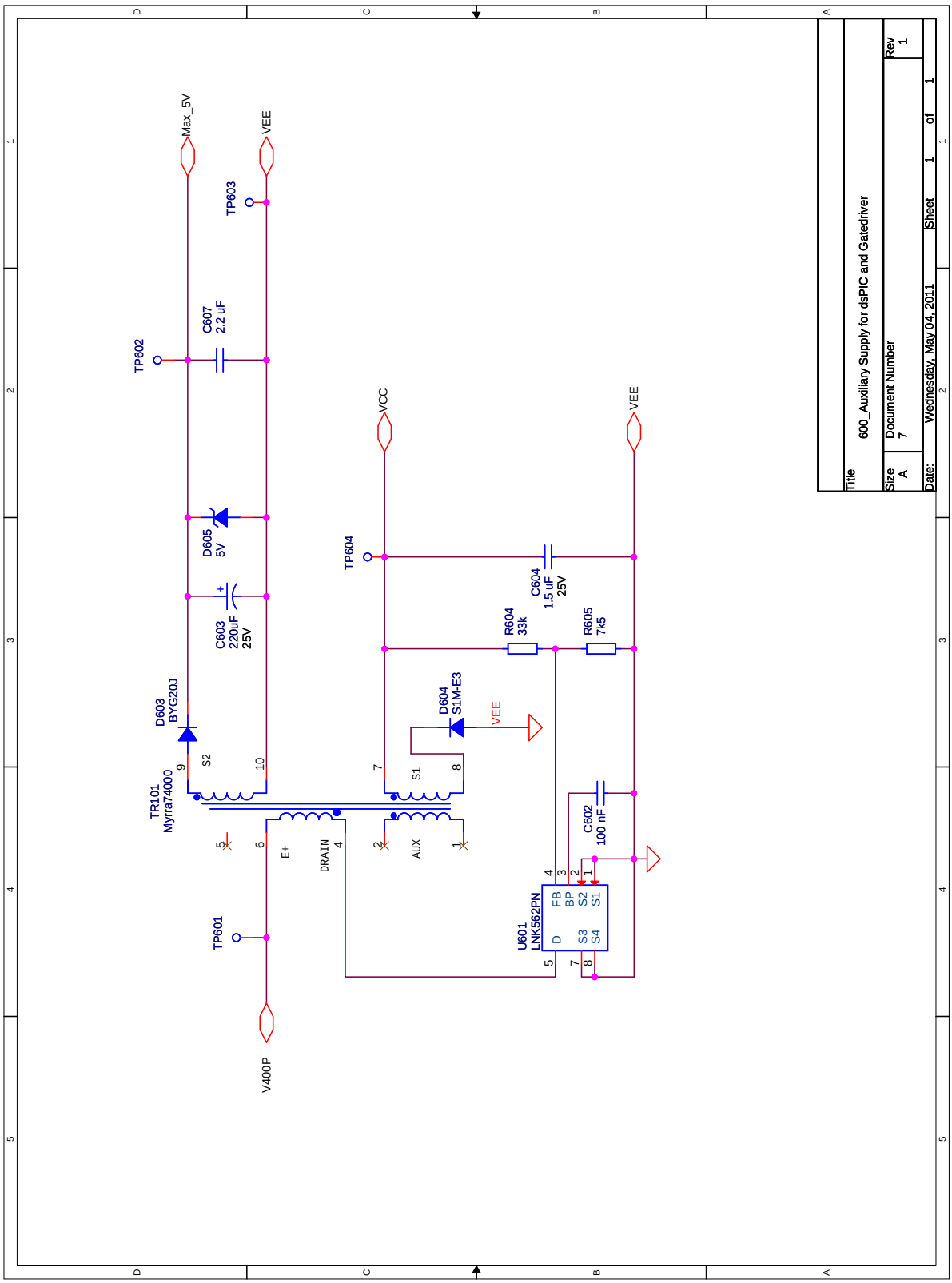

Figure B.4: *Auxiliary power supply schematic*

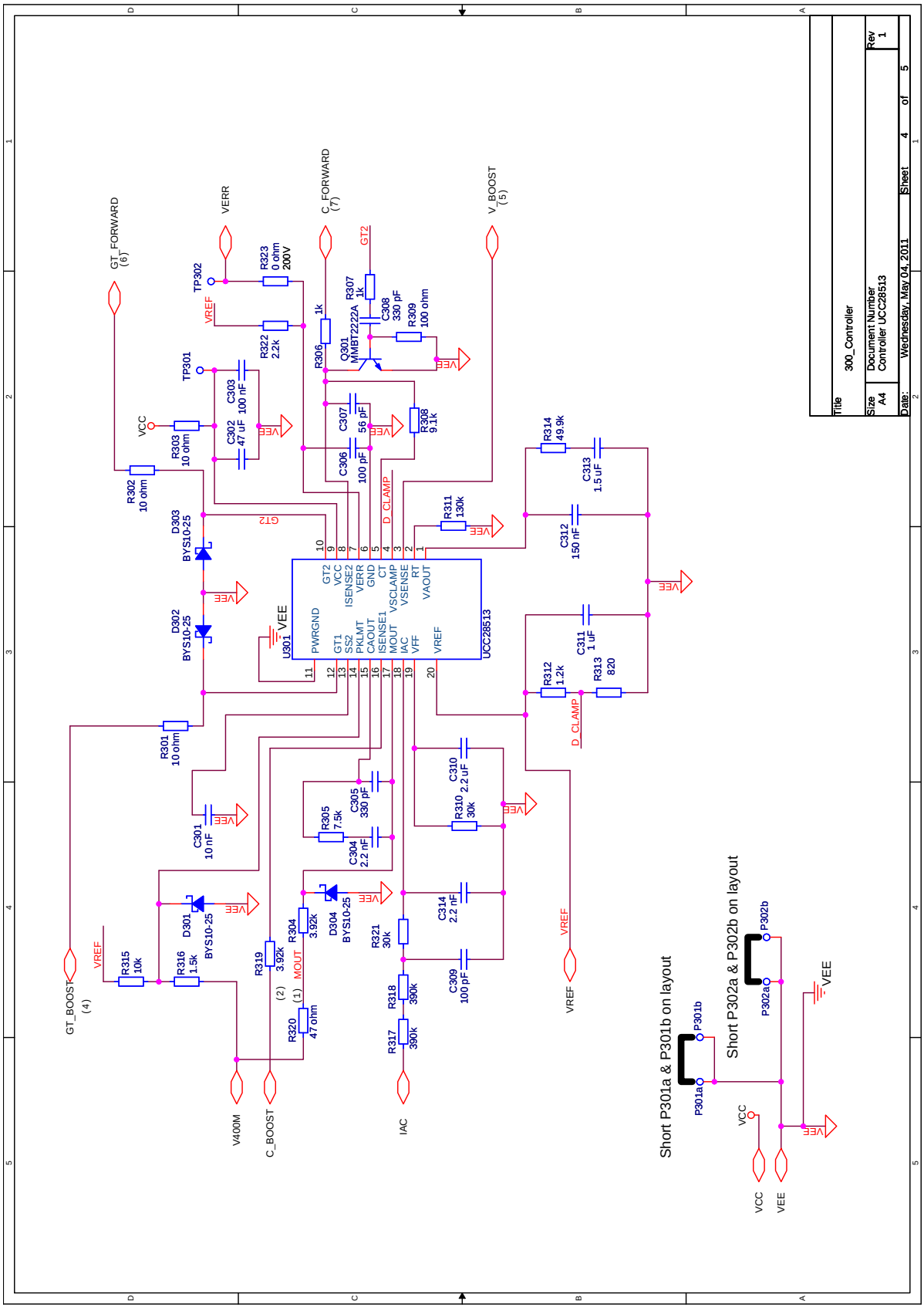

Figure B.5: *Analog controller - UCC2851x - schematic*

B.2 600 W converter schematics

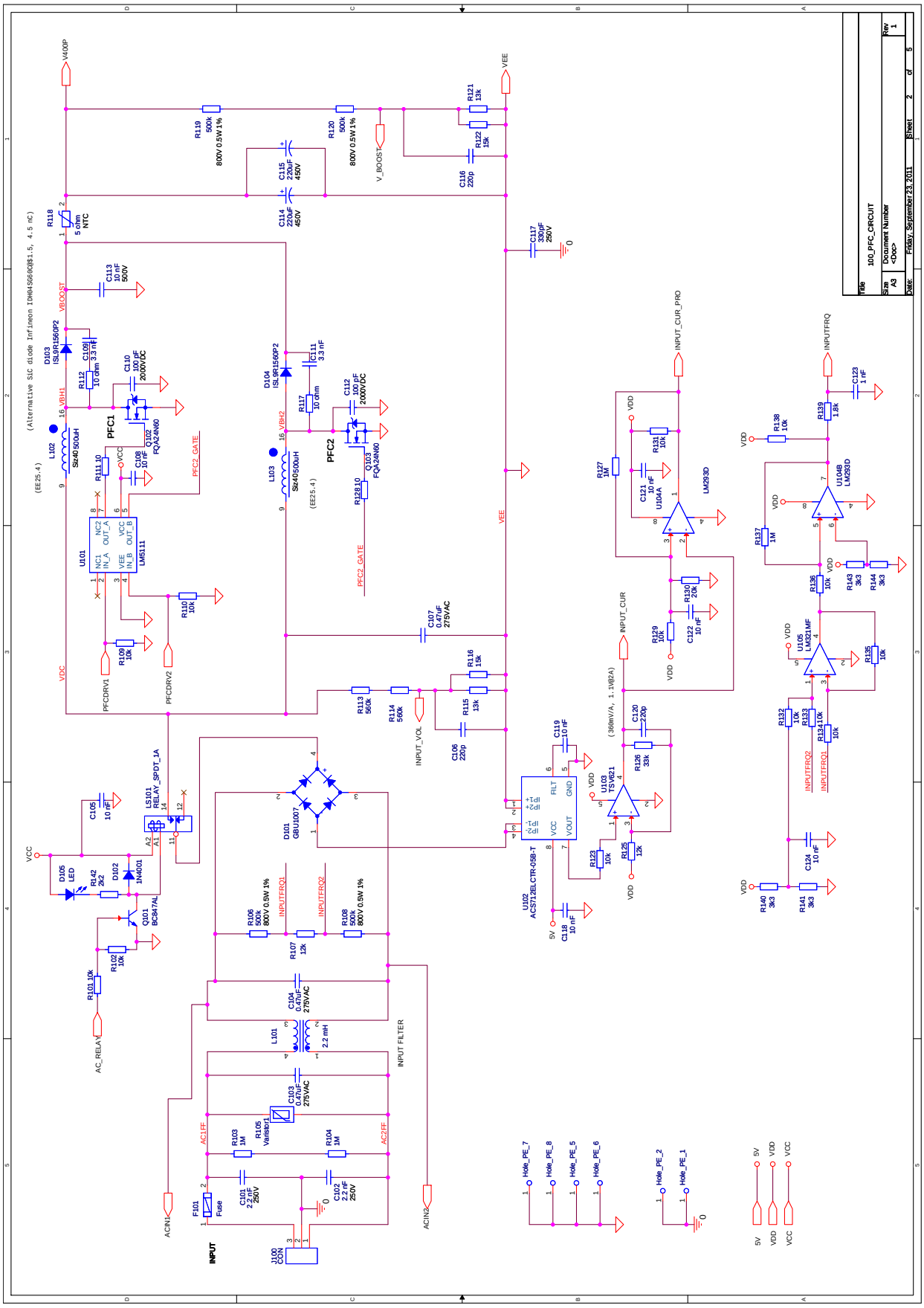

Figure B.6: *Interleaved boost converter schematic*

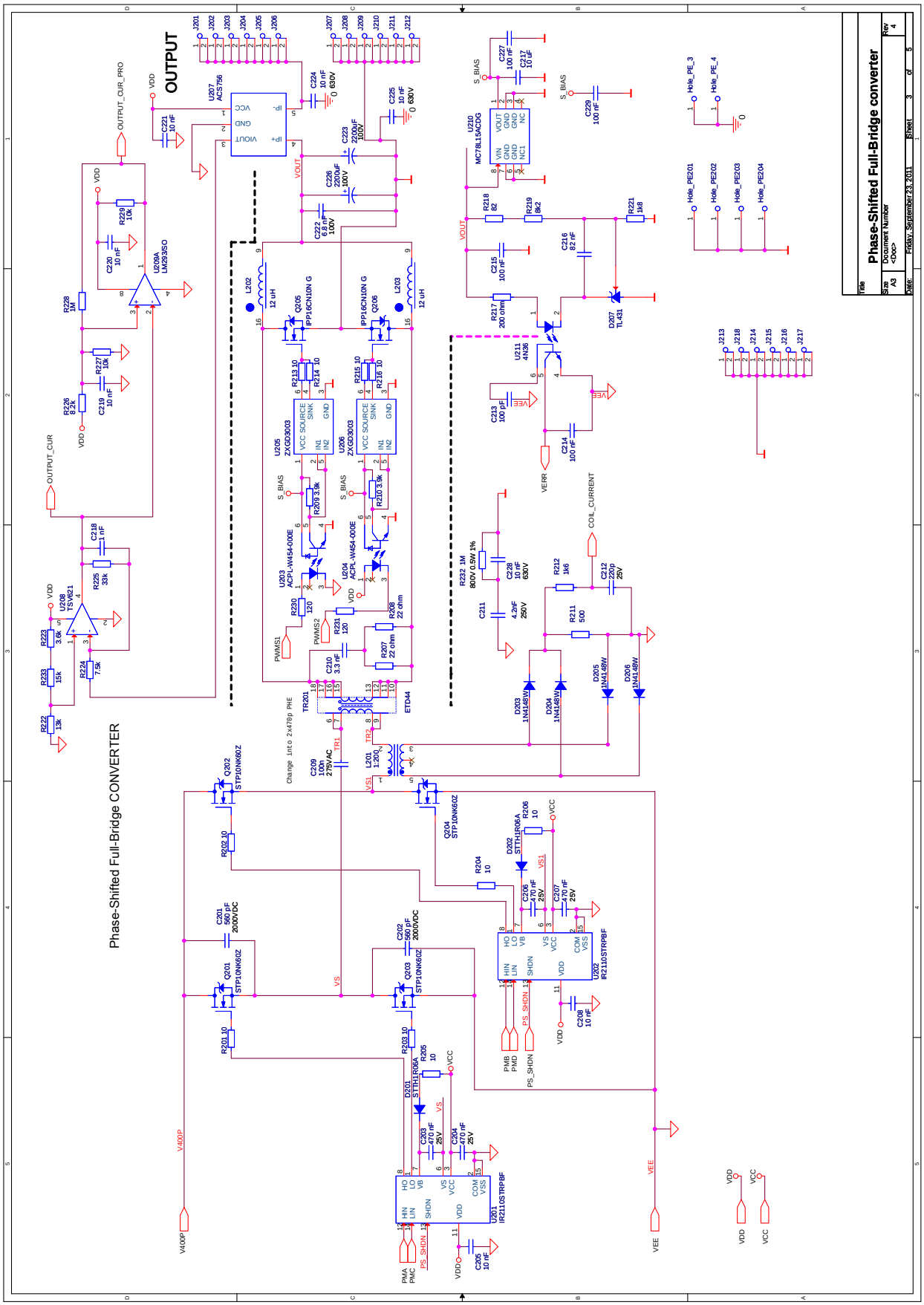

Figure B.7: *PSFB converter with synchronous rectification and current doubler schematic*

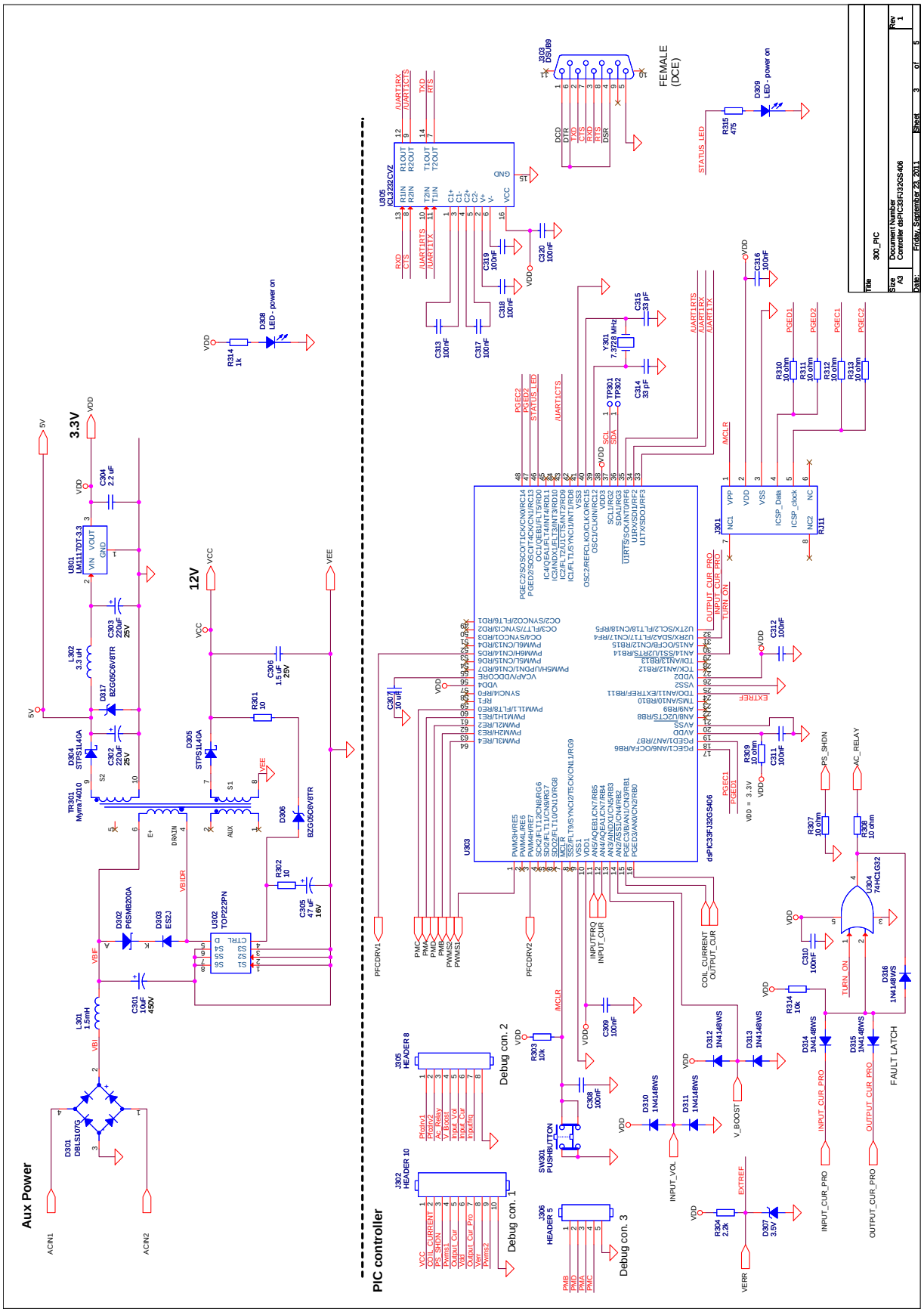

Figure B.8: *Auxiliary power supply and dsPIC connections - dsPIC33FJ32GS406 schematic*

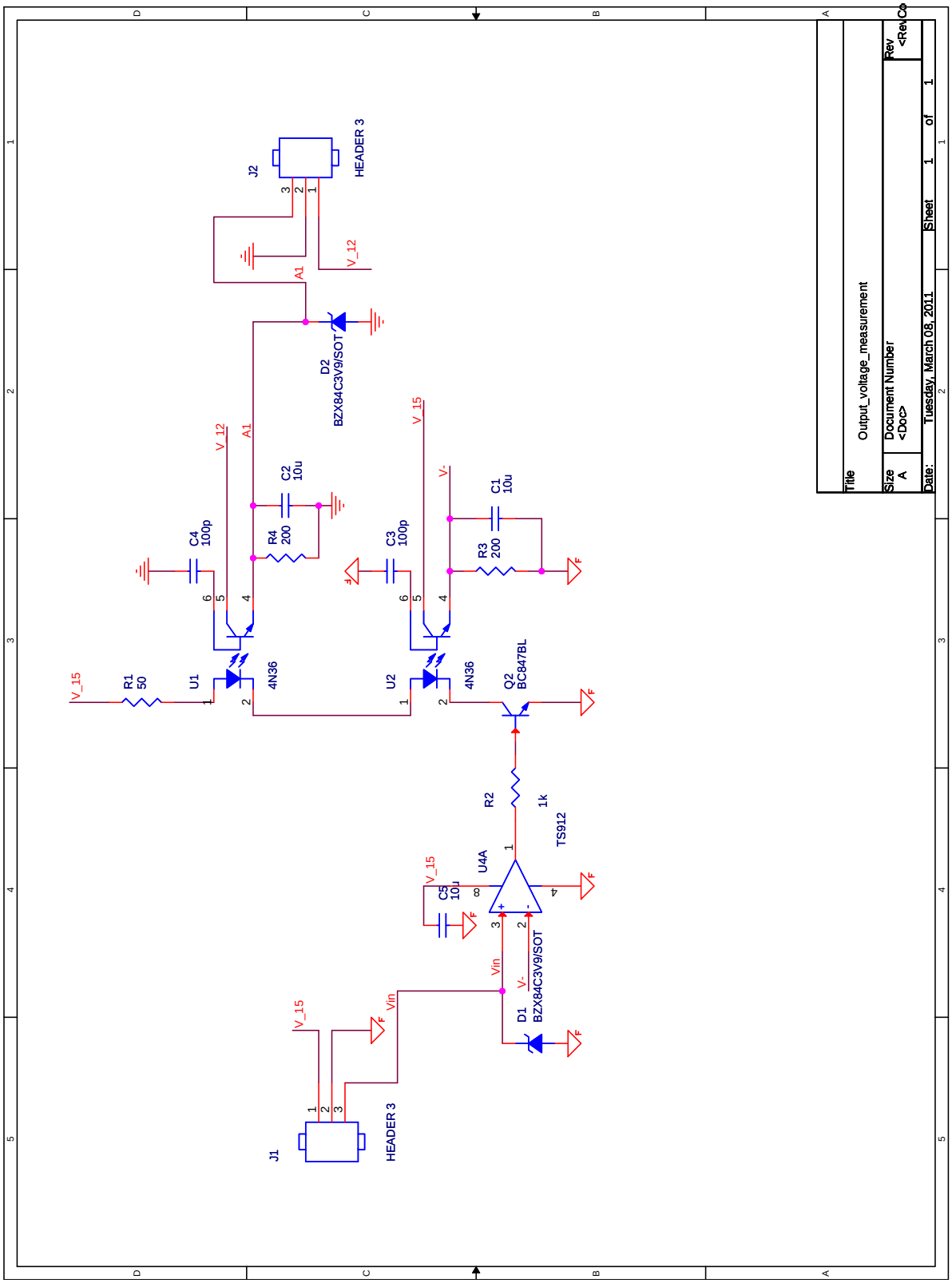

Figure B.9: *Voltage feedback with optical isolation schematic*